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ILI9342

a-Si TFT LCD Single Chip Driver
320RGBx240 Resolution and 262K color

Specification
Preliminary

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1. Introduction

ILI9342 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 320RGBx240 dots, comprising a 960-channel source driver, a 240-channel gate driver, 172,800 bytes GRAM for graphic display data of 320RGBx240 dots, and power supply circuit.

ILI9342 supports parallel 8-/9-/16-/18-bit data bus MPU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

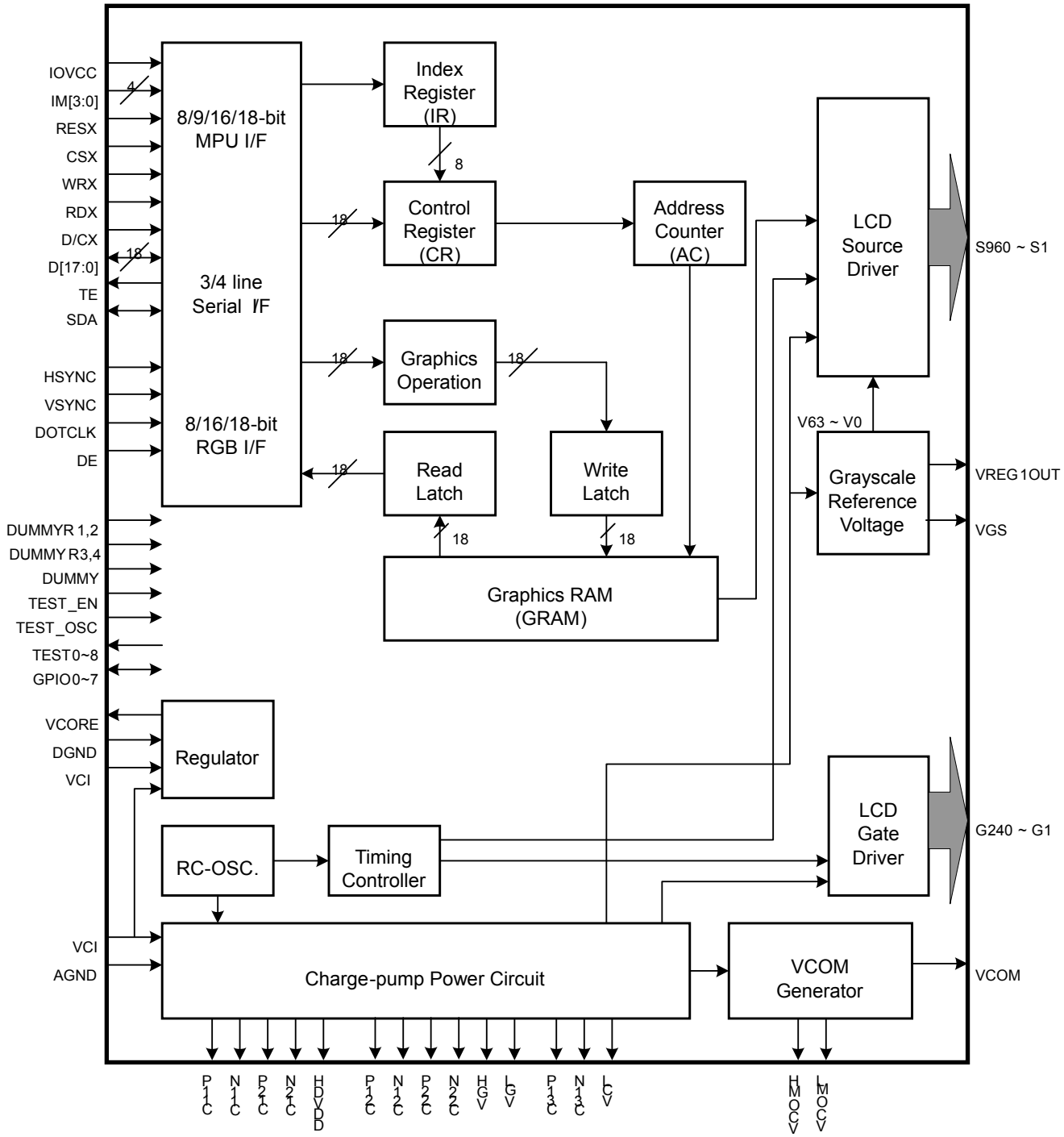
ILI9342 can operate with 1.65V ~ 3.6V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9342 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9342 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [320xRGB](H) x 240(V)
- Output:
  - 960 source outputs
  - 240 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 6800/8080-series MPU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
  - Deep standby mode
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
  - 4 preset selectable gamma curves
- MTP (3 times):
  - 8-bits for ID1, ID2, ID3
  - 7-bits for VCOM adjustment

- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC = 1.65V ~ 3.3V (logic)
    - VCI = 2.4V ~ 4.8V (analog)
- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - DDVDH - GND = 4.5V ~ 6.0V
    - VCL - GND = -2.0V ~ -3.0V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 20.0V
    - VGL - GND = -5.0V ~ -15.0V
    - VGH - VGL ≦ 32V
  - VCOM driver output voltage
    - VCOMH = 3.0V ~ (DDVDH – 0.5)V
    - VCOML = (VCL+0.5)V ~ 0V
    - VCOMH - VCOML ≦ 6.0V
- Operate temperature range: -40℃ to 85℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Block Function Description

MPU System Interface

ILI9342 provides four kinds of MPU system interface with 8080-/6800-series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MPU-Interface Mode	Pins in use
0	0	0	0	6800 MPU 8-bit bus interface	DB[7:0],R/WX,E,CSX,D/CX
0	0	0	1	6800 MPU 9-bit bus interface	DB[8:0] ,R/WX,E,CSX,D/CX
0	0	1	0	6800 MPU 16-bit bus interface	DB[15:0] ,R/WX,E,CSX,D/CX
0	0	1	1	6800 MPU 18-bit bus interface	DB[17:0] ,R/WX,E,CSX,D/CX
0	1	0	0	8080 MPU 8-bit bus interface	DB[7:0],WRX,RDX,CSX,D/CX
0	1	0	1	8080 MPU 9-bit bus interface	DB[8:0] ,WRX,RDX,CSX,D/CX
0	1	1	0	8080 MPU 16-bit bus interface	DB[15:0] ,WRX,RDX,CSX,D/CX
0	1	1	1	8080 MPU 18-bit bus interface	DB[17:0] ,WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface	SCL,SDA,CSX
1	1	1	1	4-wire 8-bit data serial interface	SCL,SDA,D/CX,CSX

In 8080-/6800-series parallel interface, the registers are accessed by the DB[7:0] data pins.

6800-Series								8080-Series				Operation
Clocked E Mode				Fixed E Mode								
CSX	D/CX	R/WX	E	CSX	D/CX	R/WX	E	CSX	D/CX	RDX	WRX	
“L”	“L”	“L”	↓	↑	“L”	“L”	“H”	“L”	“L”	“H”	↑	Write command
“L”	“H”	“H”	↓	↑	“H”	“H”	“H”	“L”	“H”	↑	“H”	Read parameter
“L”	“H”	“L”	↓	↑	“H”	“L”	“H”	“L”	“H”	“H”	↑	Write parameter

Parallel RGB Interface

ILI9342 also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 320(RGB) x240 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9342 can display maximum 262,144 colors.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as VREG1OUT, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9342 incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 960-output source driver (S1~S960), 240-output gate driver (G1~G240), and VCOM signal.

5. Pin Description

<table>
<tr><th colspan="4">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>MPU
(IOVCC/DGND)</td><td>- Select the MPU interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>6800 8-bit bus interface</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>6800 9-bit bus interface</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>6800 16-bit bus interface</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>6800 18-bit bus interface</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8080 8-bit bus interface</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>8080 9-bit bus interface</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>8080 16-bit bus interface</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8080 18-bit bus interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-line SPI</td><td>SDA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-line SPI</td><td>SDA</td></tr>
<tr><td colspan="6">(Other setting is inhibited)</td></tr>
</table>
MPU Parallel interface bus and serial interface select
Fix this pin at IOVCC or DGND.</td></tr>
<tr><td>RESX</td><td>I</td><td>MPU
(IOVCC/DGND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>CSX(CSX1)</td><td>I</td><td>MPU
(IOVCC/DGND)</td><td>Chip select input pin (“Low” enable).
This pin can be permanently fixed “Low” in MPU interface mode only.
CSX and CSX1 are connected internally winthin IC.
Note : 1,2.</td></tr>
<tr><td>D/CX(D/CX_SCL1)
(SCL)</td><td>I</td><td>MPU
(IOVCC/DGND)</td><td>This pin is used to select “Data or Command” in the parallel interface or 4-wire 8-bit serial data interface.
When DCX = ’1’, data is selected.
When DCX = ’0’, command is selected.
This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
D/CX and D/CX_SCL1 are connected internally winthin IC.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>RDX (E)</td><td>I</td><td>MPU
(IOVCC/DGND)</td><td>- 8080 system (RDX): Serves as a read signal and MPU read data at the rising edge.
- 6800 system (E): Serves as a enable/disable signal for read/write operation.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>WRX
(R/WX)
(D/CX)</td><td>I</td><td>MPU
(IOVCC/DGND)</td><td>- 8080 system (WRX): Serves as a write signal and writes data at the rising edge.
- 6800 system (R/WX): Serves as a write/read control signal.
- 4-line system (D/CX): Serves as command or parameter select.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>MPU
(IOVCC/DGND)</td><td>18-bit parallel bi-directional data bus for MPU system and RGB interface mode
Fix to DGND level when not in use</td></tr>
</table>

SDA	I/O	MPU (IOVCC/DGND)	Serial data input / output and applied on the rising edge of the SCL signal. *If not used, fix this pin at IOVCC or DGND.*
TE	O	MPU (IOVCC/DGND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. *If not used, open this pin.*
DOTCLK	I	MPU (IOVCC/DGND)	Dot clock signal for RGB interface operation. *Fix to IOVCC or DGND level when not in use.*
VSYNC	I	MPU (IOVCC/DGND)	Frame synchronizing signal for RGB interface operation. *Fix to IOVCC or DGND level when not in use.*
HSYNC	I	MPU (IOVCC/DGND)	Line synchronizing signal for RGB interface operation. *Fix to IOVCC or DGND level when not in use.*
DE	I	MPU (IOVCC/DGND)	Data enable signal for RGB interface operation. *Fix to IOVCC or DGND level when not in use.*
LCD Driving Signals			
Pin Name	I/O	Type	Descriptions
S960~S1	O	Source	Source output signals.. *Leave the pin to open when not in use.*
G240~G1	O	Gate	Gate output signals. *Leave the pin to open when not in use.*
VCOM	O	TFT common electrode	Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and AGND voltage. Connect this pad to the TFT-display counter electrode.
VCOMH	O	-	- The high level of VCOM AC voltage.
VCOML	O	-	- The low level of VCOM AC voltage.
Charge-pump and Regulator Circuit			
Pin Name	I/O	Type	Descriptions
DDVDH	O	Stabilizing capacitor	Output voltage of 1st step up circuit (2 x VCI1). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization. *Note : 3.*
VGH	O	Stabilizing capacitor	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VGL	O	Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VCL	O	Stabilizing capacitor	Power supply for VCOML. VCL = 0~ - VCI1 Connect this pad with a stabilizing capacitor.
C11P, C11N C12P, C12N	P	Step-up capacitor	Connect the charge-pumping capacitor for generating DDVDH level.
C21P, C21N C22P, C22N	P	Step-up capacitor	Connect the charge-pumping capacitor for generating VGH, VGL level.
C31P, C31N	P	Step-up capacitor	Connect the charge-pumping capacitor for generating VCL level.
VREG1OUT	O	-	Reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VGS	I	Power supply	- Reference voltage input for grayscale voltage generator. - Connect an external resistor or to system ground.
Power Pads			
Pin Name	I/O	Type	Descriptions

IOVCC	I	Power supply	Power supply for interface logic circuits (1.65 ~ 3.6 V)
VCI	I	Power supply	Power supply for analog circuit blocks (2.4 ~ 3.6 V)
VCORE	O	Digital Power	Regulated Low voltage level for interface circuits. Don't apply any external power to this pad. Connect a capacitor for stabilization.
DGND	I	Digital Ground	System ground level for logic blocks
AGND	I	Analog Ground	System ground level for analog circuit blocks Connect to DGND on the FPC to prevent noise.
VPP	I	Power supply	Power supply pin used in NV memory write mode and operated at 7.0V *Leave the pin to open when not in use.*
Test Pads			
Pin Name	I/O	Type	Descriptions
TEST_EN TEST_OSC	I	DGND	TEST pin input(internal pull low), Connect to GND when not used
TESTO1~2	O	Open	TEST pin output, Leave it open when not used
TEST0~8	I	DGND	TEST pin(internal pull low), Connect to GND when not used
DUMMYR1 DUMMYR2 DUMMYR3 DUMMYR4	-	Open	Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at DGND level.When measuring an ohm resistance of the contact, do not apply any power.
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
GPIO0~7	I/O	-	Standard input/output pin As for GPIO0~7 to terminal, setting of an input and output direction is possible

Note : 1. If CSX is connected to DGND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

3. VCI1 is an internal reference voltage generated between VCI and AGND. Reference input voltage for 1st and 3rd step up circuit.

Liquid crystal power supply specifications Table

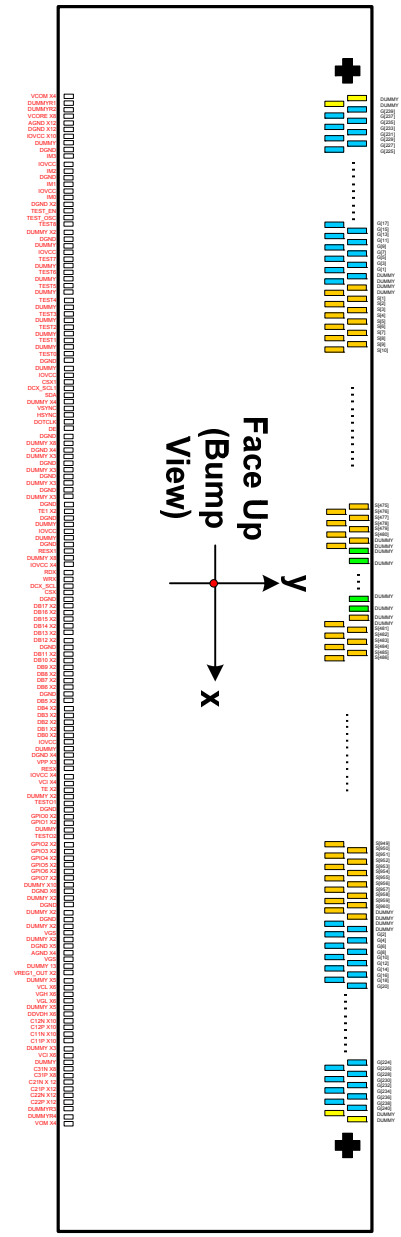
No.	Item		Description
1	TFT Source Driver		960 pins (320 x RGB)
2	TFT Gate Driver		240 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S960	V0 ~ V63 grayscales
		G1 ~ G240	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVCC	1.65V ~ 3.30V
		VCI	2.30V ~ 4.80V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10.0V ~ 20.0V
		VGL	-5.0V ~ -15.0V
		VCL	-1.9V ~ -3.0V
		VGH - VGL	Max. 32.0V
7	Internal Step-up Circuits	DDVDH	VCI1 x2, x3
		VGH	VCI1 x4, x5, x6, x7, x9
		VGL	VCI1 x-3, x-4, x-5, x-6, x-7
		VCL	VCI1 x-1

6. Pad Arrangement and Coordination

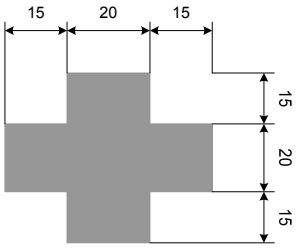
Chip Size: 18620um x 700um
Chip thickness : 280um (typ.)
Pad Location: Pad Center.
Coordinate Origin: Chip center
Au bump height: 12um (typ.)
Au Bump Size:

1. 24um x 69um
   input side :
   No. 1 ~ 436

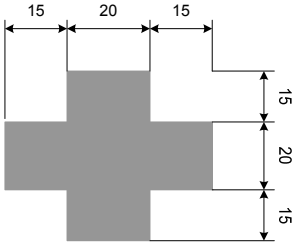
2. 14um x 110um
   Staggered LCD output side :
   No. 437 ~ 1672



Alignment Marks



Alignment Mark: A1
(-9200, 225)



Alignment Mark: A2
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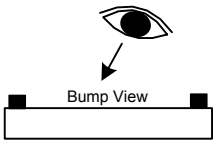


6.1 PAD Coordinate

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	VCOM	-8989	-245.5	51	IM3	-6989	-245.5	101	DUMMY	-4989	-245.5	151	DB17	-2989	-245.5
2	VCOM	-8949	-245.5	52	IOVCC	-6949	-245.5	102	DUMMY	-4949	-245.5	152	DB17	-2949	-245.5
3	VCOM	-8909	-245.5	53	IM2	-6909	-245.5	103	DUMMY	-4909	-245.5	153	DB16	-2909	-245.5
4	VCOM	-8869	-245.5	54	DGND	-6869	-245.5	104	DUMMY	-4869	-245.5	154	DB16	-2869	-245.5
5	DUMMYR1	-8829	-245.5	55	IM1	-6829	-245.5	105	DUMMY	-4829	-245.5	155	DB15	-2829	-245.5
6	DUMMYR2	-8789	-245.5	56	IOVCC	-6789	-245.5	106	DGND	-4789	-245.5	156	DB15	-2789	-245.5
7	VCORE	-8749	-245.5	57	IM0	-6749	-245.5	107	DGND	-4749	-245.5	157	DB14	-2749	-245.5
8	VCORE	-8709	-245.5	58	DGND	-6709	-245.5	108	DGND	-4709	-245.5	158	DB14	-2709	-245.5
9	VCORE	-8669	-245.5	59	DGND	-6669	-245.5	109	DGND	-4669	-245.5	159	DB13	-2669	-245.5
10	VCORE	-8629	-245.5	60	TEST_EN	-6629	-245.5	110	DUMMY	-4629	-245.5	160	DB13	-2629	-245.5
11	VCORE	-8589	-245.5	61	TEST_OSC	-6589	-245.5	111	DUMMY	-4589	-245.5	161	DB12	-2589	-245.5
12	VCORE	-8549	-245.5	62	TEST8	-6549	-245.5	112	DUMMY	-4549	-245.5	162	DB12	-2549	-245.5
13	VCORE	-8509	-245.5	63	DUMMY	-6509	-245.5	113	DGND	-4509	-245.5	163	DGND	-2509	-245.5
14	VCORE	-8469	-245.5	64	DUMMY	-6469	-245.5	114	DUMMY	-4469	-245.5	164	DB11	-2469	-245.5
15	AGND	-8429	-245.5	65	DGND	-6429	-245.5	115	DUMMY	-4429	-245.5	165	DB11	-2429	-245.5
16	AGND	-8389	-245.5	66	DUMMY	-6389	-245.5	116	DUMMY	-4389	-245.5	166	DB10	-2389	-245.5
17	AGND	-8349	-245.5	67	IOVCC	-6349	-245.5	117	DGND	-4349	-245.5	167	DB10	-2349	-245.5
18	AGND	-8309	-245.5	68	TEST7	-6309	-245.5	118	DUMMY	-4309	-245.5	168	DB9	-2309	-245.5
19	AGND	-8269	-245.5	69	DUMMY	-6269	-245.5	119	DUMMY	-4269	-245.5	169	DB9	-2269	-245.5
20	AGND	-8229	-245.5	70	TEST6	-6229	-245.5	120	DUMMY	-4229	-245.5	170	DB8	-2229	-245.5
21	AGND	-8189	-245.5	71	DUMMY	-6189	-245.5	121	DGND	-4189	-245.5	171	DB8	-2189	-245.5
22	AGND	-8149	-245.5	72	TEST5	-6149	-245.5	122	DUMMY	-4149	-245.5	172	DB7	-2149	-245.5
23	AGND	-8109	-245.5	73	DUMMY	-6109	-245.5	123	DUMMY	-4109	-245.5	173	DB7	-2109	-245.5
24	AGND	-8069	-245.5	74	TEST4	-6069	-245.5	124	DUMMY	-4069	-245.5	174	DB6	-2069	-245.5
25	AGND	-8029	-245.5	75	DUMMY	-6029	-245.5	125	DGND	-4029	-245.5	175	DB6	-2029	-245.5
26	AGND	-7989	-245.5	76	TEST3	-5989	-245.5	126	TE1	-3989	-245.5	176	DGND	-1989	-245.5
27	DGND	-7949	-245.5	77	DUMMY	-5949	-245.5	127	TE1	-3949	-245.5	177	DB5	-1949	-245.5
28	DGND	-7909	-245.5	78	TEST2	-5909	-245.5	128	DGND	-3909	-245.5	178	DB5	-1909	-245.5
29	DGND	-7869	-245.5	79	DUMMY	-5869	-245.5	129	DUMMY	-3869	-245.5	179	DB4	-1869	-245.5
30	DGND	-7829	-245.5	80	TEST1	-5829	-245.5	130	IOVCC	-3829	-245.5	180	DB4	-1829	-245.5
31	DGND	-7789	-245.5	81	DUMMY	-5789	-245.5	131	DUMMY	-3789	-245.5	181	DB3	-1789	-245.5
32	DGND	-7749	-245.5	82	TEST0	-5749	-245.5	132	DGND	-3749	-245.5	182	DB3	-1749	-245.5
33	DGND	-7709	-245.5	83	DGND	-5709	-245.5	133	RESX1	-3709	-245.5	183	DB2	-1709	-245.5
34	DGND	-7669	-245.5	84	DUMMY	-5669	-245.5	134	DUMMY	-3669	-245.5	184	DB2	-1669	-245.5
35	DGND	-7629	-245.5	85	IOVCC	-5629	-245.5	135	DUMMY	-3629	-245.5	185	DB1	-1629	-245.5
36	DGND	-7589	-245.5	86	CSX1	-5589	-245.5	136	DUMMY	-3589	-245.5	186	DB1	-1589	-245.5
37	DGND	-7549	-245.5	87	DCX_SCL1	-5549	-245.5	137	DUMMY	-3549	-245.5	187	DB0	-1549	-245.5
38	DGND	-7509	-245.5	88	SDA	-5509	-245.5	138	DUMMY	-3509	-245.5	188	DB0	-1509	-245.5
39	IOVCC	-7469	-245.5	89	DUMMY	-5469	-245.5	139	DUMMY	-3469	-245.5	189	IOVCC	-1469	-245.5
40	IOVCC	-7429	-245.5	90	DUMMY	-5429	-245.5	140	DUMMY	-3429	-245.5	190	DUMMY	-1429	-245.5
41	IOVCC	-7389	-245.5	91	DUMMY	-5389	-245.5	141	DUMMY	-3389	-245.5	191	DGND	-1389	-245.5
42	IOVCC	-7349	-245.5	92	DUMMY	-5349	-245.5	142	IOVCC	-3349	-245.5	192	DGND	-1349	-245.5
43	IOVCC	-7309	-245.5	93	VSYNC	-5309	-245.5	143	IOVCC	-3309	-245.5	193	DGND	-1309	-245.5
44	IOVCC	-7269	-245.5	94	HSYNC	-5269	-245.5	144	IOVCC	-3269	-245.5	194	DGND	-1269	-245.5
45	IOVCC	-7229	-245.5	95	DOTCLK	-5229	-245.5	145	IOVCC	-3229	-245.5	195	VPP	-1229	-245.5
46	IOVCC	-7189	-245.5	96	DE	-5189	-245.5	146	RDX	-3189	-245.5	196	VPP	-1189	-245.5
47	IOVCC	-7149	-245.5	97	DGND	-5149	-245.5	147	WRX	-3149	-245.5	197	VPP	-1149	-245.5
48	IOVCC	-7109	-245.5	98	DUMMY	-5109	-245.5	148	DCX_SCL	-3109	-245.5	198	RESX	-1109	-245.5
49	DUMMY	-7069	-245.5	99	DUMMY	-5069	-245.5	149	CSX	-3069	-245.5	199	IOVCC	-1069	-245.5
50	DGND	-7029	-245.5	100	DUMMY	-5029	-245.5	150	DGND	-3029	-245.5	200	IOVCC	-1029	-245.5

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
201	IOVCC	-989	-245.5	251	DUMMY	1589	-245.5	301	VGL	3589	-245.5	351	C11P	5589	-245.5
202	IOVCC	-949	-245.5	252	DGND	1629	-245.5	302	VGL	3629	-245.5	352	C11P	5629	-245.5
203	VCI	-909	-245.5	253	DUMMY	1669	-245.5	303	VGL	3669	-245.5	353	C11P	5669	-245.5
204	VCI	-869	-245.5	254	DUMMY	1709	-245.5	304	VGL	3709	-245.5	354	C11P	5709	-245.5
205	VCI	-829	-245.5	255	VGS	1749	-245.5	305	VGL	3749	-245.5	355	C11P	5749	-245.5
206	VCI	-789	-245.5	256	DUMMY	1789	-245.5	306	DUMMY	3789	-245.5	356	C11P	5789	-245.5
207	TE	-749	-245.5	257	DUMMY	1829	-245.5	307	DUMMY	3829	-245.5	357	DUMMY	5829	-245.5
208	TE	-709	-245.5	258	DGND	1869	-245.5	308	DUMMY	3869	-245.5	358	DUMMY	5869	-245.5
209	DUMMY	-669	-245.5	259	DGND	1909	-245.5	309	DUMMY	3909	-245.5	359	DUMMY	5909	-245.5
210	DUMMY	-629	-245.5	260	DGND	1949	-245.5	310	DUMMY	3949	-245.5	360	VCI	5949	-245.5
211	TESTO1	-589	-245.5	261	DGND	1989	-245.5	311	DDVDH	3989	-245.5	361	VCI	5989	-245.5
212	DGND	-549	-245.5	262	DGND	2029	-245.5	312	DDVDH	4029	-245.5	362	VCI	6029	-245.5
213	GPIO0	-509	-245.5	263	AGND	2069	-245.5	313	DDVDH	4069	-245.5	363	VCI	6069	-245.5
214	GPIO0	-469	-245.5	264	AGND	2109	-245.5	314	DDVDH	4109	-245.5	364	VCI	6109	-245.5
215	GPIO1	-429	-245.5	265	AGND	2149	-245.5	315	DDVDH	4149	-245.5	365	VCI	6149	-245.5
216	GPIO1	-389	-245.5	266	AGND	2189	-245.5	316	DDVDH	4189	-245.5	366	DUMMY	6189	-245.5
217	DUMMY	-349	-245.5	267	VGS	2229	-245.5	317	C12N	4229	-245.5	367	C31N	6229	-245.5
218	TESTO2	-309	-245.5	268	DUMMY	2269	-245.5	318	C12N	4269	-245.5	368	C31N	6269	-245.5
219	GPIO2	309	-245.5	269	DUMMY	2309	-245.5	319	C12N	4309	-245.5	369	C31N	6309	-245.5
220	GPIO2	349	-245.5	270	DUMMY	2349	-245.5	320	C12N	4349	-245.5	370	C31N	6349	-245.5
221	GPIO3	389	-245.5	271	DUMMY	2389	-245.5	321	C12N	4389	-245.5	371	C31N	6389	-245.5
222	GPIO3	429	-245.5	272	DUMMY	2429	-245.5	322	C12N	4429	-245.5	372	C31N	6429	-245.5
223	GPIO4	469	-245.5	273	DUMMY	2469	-245.5	323	C12N	4469	-245.5	373	C31N	6469	-245.5
224	GPIO4	509	-245.5	274	DUMMY	2509	-245.5	324	C12N	4509	-245.5	374	C31N	6509	-245.5
225	GPIO5	549	-245.5	275	DUMMY	2549	-245.5	325	C12N	4549	-245.5	375	C31P	6549	-245.5
226	GPIO5	589	-245.5	276	DUMMY	2589	-245.5	326	C12N	4589	-245.5	376	C31P	6589	-245.5
227	GPIO6	629	-245.5	277	DUMMY	2629	-245.5	327	C12P	4629	-245.5	377	C31P	6629	-245.5
228	GPIO6	669	-245.5	278	DUMMY	2669	-245.5	328	C12P	4669	-245.5	378	C31P	6669	-245.5
229	GPIO7	709	-245.5	279	DUMMY	2709	-245.5	329	C12P	4709	-245.5	379	C31P	6709	-245.5
230	GPIO7	749	-245.5	280	DUMMY	2749	-245.5	330	C12P	4749	-245.5	380	C31P	6749	-245.5
231	DUMMY	789	-245.5	281	VREG1_OUT	2789	-245.5	331	C12P	4789	-245.5	381	C31P	6789	-245.5
232	DUMMY	829	-245.5	282	VREG1_OUT	2829	-245.5	332	C12P	4829	-245.5	382	C31P	6829	-245.5
233	DUMMY	869	-245.5	283	DUMMY	2869	-245.5	333	C12P	4869	-245.5	383	C21N	6869	-245.5
234	DUMMY	909	-245.5	284	DUMMY	2909	-245.5	334	C12P	4909	-245.5	384	C21N	6909	-245.5
235	DUMMY	949	-245.5	285	DUMMY	2949	-245.5	335	C12P	4949	-245.5	385	C21N	6949	-245.5
236	DUMMY	989	-245.5	286	DUMMY	2989	-245.5	336	C12P	4989	-245.5	386	C21N	6989	-245.5
237	DUMMY	1029	-245.5	287	DUMMY	3029	-245.5	337	C11N	5029	-245.5	387	C21N	7029	-245.5
238	DUMMY	1069	-245.5	288	VCL	3069	-245.5	338	C11N	5069	-245.5	388	C21N	7069	-245.5
239	DUMMY	1109	-245.5	289	VCL	3109	-245.5	339	C11N	5109	-245.5	389	C21N	7109	-245.5
240	DUMMY	1149	-245.5	290	VCL	3149	-245.5	340	C11N	5149	-245.5	390	C21N	7149	-245.5
241	DGND	1189	-245.5	291	VCL	3189	-245.5	341	C11N	5189	-245.5	391	C21N	7189	-245.5
242	DGND	1229	-245.5	292	VCL	3229	-245.5	342	C11N	5229	-245.5	392	C21N	7229	-245.5
243	DGND	1269	-245.5	293	VCL	3269	-245.5	343	C11N	5269	-245.5	393	C21N	7269	-245.5
244	DGND	1309	-245.5	294	VGH	3309	-245.5	344	C11N	5309	-245.5	394	C21N	7309	-245.5
245	DGND	1349	-245.5	295	VGH	3349	-245.5	345	C11N	5349	-245.5	395	C21P	7349	-245.5
246	DGND	1389	-245.5	296	VGH	3389	-245.5	346	C11N	5389	-245.5	396	C21P	7389	-245.5
247	DUMMY	1429	-245.5	297	VGH	3429	-245.5	347	C11P	5429	-245.5	397	C21P	7429	-245.5
248	DUMMY	1469	-245.5	298	VGH	3469	-245.5	348	C11P	5469	-245.5	398	C21P	7469	-245.5
249	DGND	1509	-245.5	299	VGH	3509	-245.5	349	C11P	5509	-245.5	399	C21P	7509	-245.5
250	DUMMY	1549	-245.5	300	VGL	3549	-245.5	350	C11P	5549	-245.5	400	C21P	7549	-245.5

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
401	C21P	7589	-245.5	451	G216	8811	223	501	G116	8011	223	551	G16	7211	223
402	C21P	7629	-245.5	452	G214	8795	97	502	G114	7995	97	552	G14	7195	97
403	C21P	7669	-245.5	453	G212	8779	223	503	G112	7979	223	553	G12	7179	223
404	C21P	7709	-245.5	454	G210	8763	97	504	G110	7963	97	554	G10	7163	97
405	C21P	7749	-245.5	455	G208	8747	223	505	G108	7947	223	555	G8	7147	223
406	C21P	7789	-245.5	456	G206	8731	97	506	G106	7931	97	556	G6	7131	97
407	C22N	7829	-245.5	457	G204	8715	223	507	G104	7915	223	557	G4	7115	223
408	C22N	7869	-245.5	458	G202	8699	97	508	G102	7899	97	558	G2	7099	97
409	C22N	7909	-245.5	459	G200	8683	223	509	G100	7883	223	559	DUMMY	7083	223
410	C22N	7949	-245.5	460	G198	8667	97	510	G98	7867	97	560	DUMMY	7067	97
411	C22N	7989	-245.5	461	G196	8651	223	511	G96	7851	223	561	DUMMY	7051	223
412	C22N	8029	-245.5	462	G194	8635	97	512	G94	7835	97	562	DUMMY	7037	97
413	C22N	8069	-245.5	463	G192	8619	223	513	G92	7819	223	563	S960	7023	223
414	C22N	8109	-245.5	464	G190	8603	97	514	G90	7803	97	564	S959	7009	97
415	C22N	8149	-245.5	465	G188	8587	223	515	G88	7787	223	565	S958	6995	223
416	C22N	8189	-245.5	466	G186	8571	97	516	G86	7771	97	566	S957	6981	97
417	C22N	8229	-245.5	467	G184	8555	223	517	G84	7755	223	567	S956	6967	223
418	C22N	8269	-245.5	468	G182	8539	97	518	G82	7739	97	568	S955	6953	97
419	C22P	8309	-245.5	469	G180	8523	223	519	G80	7723	223	569	S954	6939	223
420	C22P	8349	-245.5	470	G178	8507	97	520	G78	7707	97	570	S953	6925	97
421	C22P	8389	-245.5	471	G176	8491	223	521	G76	7691	223	571	S952	6911	223
422	C22P	8429	-245.5	472	G174	8475	97	522	G74	7675	97	572	S951	6897	97
423	C22P	8469	-245.5	473	G172	8459	223	523	G72	7659	223	573	S950	6883	223
424	C22P	8509	-245.5	474	G170	8443	97	524	G70	7643	97	574	S949	6869	97
425	C22P	8549	-245.5	475	G168	8427	223	525	G68	7627	223	575	S948	6855	223
426	C22P	8589	-245.5	476	G166	8411	97	526	G66	7611	97	576	S947	6841	97
427	C22P	8629	-245.5	477	G164	8395	223	527	G64	7595	223	577	S946	6827	223
428	C22P	8669	-245.5	478	G162	8379	97	528	G62	7579	97	578	S945	6813	97
429	C22P	8709	-245.5	479	G160	8363	223	529	G60	7563	223	579	S944	6799	223
430	C22P	8749	-245.5	480	G158	8347	97	530	G58	7547	97	580	S943	6785	97
431	DUMMYR3	8789	-245.5	481	G156	8331	223	531	G56	7531	223	581	S942	6771	223
432	DUMMYR4	8829	-245.5	482	G154	8315	97	532	G54	7515	97	582	S941	6757	97
433	VCOM	8869	-245.5	483	G152	8299	223	533	G52	7499	223	583	S940	6743	223
434	VCOM	8909	-245.5	484	G150	8283	97	534	G50	7483	97	584	S939	6729	97
435	VCOM	8949	-245.5	485	G148	8267	223	535	G48	7467	223	585	S938	6715	223
436	VCOM	8989	-245.5	486	G146	8251	97	536	G46	7451	97	586	S937	6701	97
437	DUMMY	9035	223	487	G144	8235	223	537	G44	7435	223	587	S936	6687	223
438	DUMMY	9019	97	488	G142	8219	97	538	G42	7419	97	588	S935	6673	97
439	G240	9003	223	489	G140	8203	223	539	G40	7403	223	589	S934	6659	223
440	G238	8987	97	490	G138	8187	97	540	G38	7387	97	590	S933	6645	97
441	G236	8971	223	491	G136	8171	223	541	G36	7371	223	591	S932	6631	223
442	G234	8955	97	492	G134	8155	97	542	G34	7355	97	592	S931	6617	97
443	G232	8939	223	493	G132	8139	223	543	G32	7339	223	593	S930	6603	223
444	G230	8923	97	494	G130	8123	97	544	G30	7323	97	594	S929	6589	97
445	G228	8907	223	495	G128	8107	223	545	G28	7307	223	595	S928	6575	223
446	G226	8891	97	496	G126	8091	97	546	G26	7291	97	596	S927	6561	97
447	G224	8875	223	497	G124	8075	223	547	G24	7275	223	597	S926	6547	223
448	G222	8859	97	498	G122	8059	97	548	G22	7259	97	598	S925	6533	97
449	G220	8843	223	499	G120	8043	223	549	G20	7243	223	599	S924	6519	223
450	G218	8827	97	500	G118	8027	97	550	G18	7227	97	600	S923	6505	97

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
601	S922	6491	223	651	S872	5791	223	701	S822	5091	223	751	S772	4391	223
602	S921	6477	97	652	S871	5777	97	702	S821	5077	97	752	S771	4377	97
603	S920	6463	223	653	S870	5763	223	703	S820	5063	223	753	S770	4363	223
604	S919	6449	97	654	S869	5749	97	704	S819	5049	97	754	S769	4349	97
605	S918	6435	223	655	S868	5735	223	705	S818	5035	223	755	S768	4335	223
606	S917	6421	97	656	S867	5721	97	706	S817	5021	97	756	S767	4321	97
607	S916	6407	223	657	S866	5707	223	707	S816	5007	223	757	S766	4307	223
608	S915	6393	97	658	S865	5693	97	708	S815	4993	97	758	S765	4293	97
609	S914	6379	223	659	S864	5679	223	709	S814	4979	223	759	S764	4279	223
610	S913	6365	97	660	S863	5665	97	710	S813	4965	97	760	S763	4265	97
611	S912	6351	223	661	S862	5651	223	711	S812	4951	223	761	S762	4251	223
612	S911	6337	97	662	S861	5637	97	712	S811	4937	97	762	S761	4237	97
613	S910	6323	223	663	S860	5623	223	713	S810	4923	223	763	S760	4223	223
614	S909	6309	97	664	S859	5609	97	714	S809	4909	97	764	S759	4209	97
615	S908	6295	223	665	S858	5595	223	715	S808	4895	223	765	S758	4195	223
616	S907	6281	97	666	S857	5581	97	716	S807	4881	97	766	S757	4181	97
617	S906	6267	223	667	S856	5567	223	717	S806	4867	223	767	S756	4167	223
618	S905	6253	97	668	S855	5553	97	718	S805	4853	97	768	S755	4153	97
619	S904	6239	223	669	S854	5539	223	719	S804	4839	223	769	S754	4139	223
620	S903	6225	97	670	S853	5525	97	720	S803	4825	97	770	S753	4125	97
621	S902	6211	223	671	S852	5511	223	721	S802	4811	223	771	S752	4111	223
622	S901	6197	97	672	S851	5497	97	722	S801	4797	97	772	S751	4097	97
623	S900	6183	223	673	S850	5483	223	723	S800	4783	223	773	S750	4083	223
624	S899	6169	97	674	S849	5469	97	724	S799	4769	97	774	S749	4069	97
625	S898	6155	223	675	S848	5455	223	725	S798	4755	223	775	S748	4055	223
626	S897	6141	97	676	S847	5441	97	726	S797	4741	97	776	S747	4041	97
627	S896	6127	223	677	S846	5427	223	727	S796	4727	223	777	S746	4027	223
628	S895	6113	97	678	S845	5413	97	728	S795	4713	97	778	S745	4013	97
629	S894	6099	223	679	S844	5399	223	729	S794	4699	223	779	S744	3999	223
630	S893	6085	97	680	S843	5385	97	730	S793	4685	97	780	S743	3985	97
631	S892	6071	223	681	S842	5371	223	731	S792	4671	223	781	S742	3971	223
632	S891	6057	97	682	S841	5357	97	732	S791	4657	97	782	S741	3957	97
633	S890	6043	223	683	S840	5343	223	733	S790	4643	223	783	S740	3943	223
634	S889	6029	97	684	S839	5329	97	734	S789	4629	97	784	S739	3929	97
635	S888	6015	223	685	S838	5315	223	735	S788	4615	223	785	S738	3915	223
636	S887	6001	97	686	S837	5301	97	736	S787	4601	97	786	S737	3901	97
637	S886	5987	223	687	S836	5287	223	737	S786	4587	223	787	S736	3887	223
638	S885	5973	97	688	S835	5273	97	738	S785	4573	97	788	S735	3873	97
639	S884	5959	223	689	S834	5259	223	739	S784	4559	223	789	S734	3859	223
640	S883	5945	97	690	S833	5245	97	740	S783	4545	97	790	S733	3845	97
641	S882	5931	223	691	S832	5231	223	741	S782	4531	223	791	S732	3831	223
642	S881	5917	97	692	S831	5217	97	742	S781	4517	97	792	S731	3817	97
643	S880	5903	223	693	S830	5203	223	743	S780	4503	223	793	S730	3803	223
644	S879	5889	97	694	S829	5189	97	744	S779	4489	97	794	S729	3789	97
645	S878	5875	223	695	S828	5175	223	745	S778	4475	223	795	S728	3775	223
646	S877	5861	97	696	S827	5161	97	746	S777	4461	97	796	S727	3761	97
647	S876	5847	223	697	S826	5147	223	747	S776	4447	223	797	S726	3747	223
648	S875	5833	97	698	S825	5133	97	748	S775	4433	97	798	S725	3733	97
649	S874	5819	223	699	S824	5119	223	749	S774	4419	223	799	S724	3719	223
650	S873	5805	97	700	S823	5105	97	750	S773	4405	97	800	S723	3705	97

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
801	S722	3691	223	851	S672	2991	223	901	S622	2291	223	951	S572	1591	223
802	S721	3677	97	852	S671	2977	97	902	S621	2277	97	952	S571	1577	97
803	S720	3663	223	853	S670	2963	223	903	S620	2263	223	953	S570	1563	223
804	S719	3649	97	854	S669	2949	97	904	S619	2249	97	954	S569	1549	97
805	S718	3635	223	855	S668	2935	223	905	S618	2235	223	955	S568	1535	223
806	S717	3621	97	856	S667	2921	97	906	S617	2221	97	956	S567	1521	97
807	S716	3607	223	857	S666	2907	223	907	S616	2207	223	957	S566	1507	223
808	S715	3593	97	858	S665	2893	97	908	S615	2193	97	958	S565	1493	97
809	S714	3579	223	859	S664	2879	223	909	S614	2179	223	959	S564	1479	223
810	S713	3565	97	860	S663	2865	97	910	S613	2165	97	960	S563	1465	97
811	S712	3551	223	861	S662	2851	223	911	S612	2151	223	961	S562	1451	223
812	S711	3537	97	862	S661	2837	97	912	S611	2137	97	962	S561	1437	97
813	S710	3523	223	863	S660	2823	223	913	S610	2123	223	963	S560	1423	223
814	S709	3509	97	864	S659	2809	97	914	S609	2109	97	964	S559	1409	97
815	S708	3495	223	865	S658	2795	223	915	S608	2095	223	965	S558	1395	223
816	S707	3481	97	866	S657	2781	97	916	S607	2081	97	966	S557	1381	97
817	S706	3467	223	867	S656	2767	223	917	S606	2067	223	967	S556	1367	223
818	S705	3453	97	868	S655	2753	97	918	S605	2053	97	968	S555	1353	97
819	S704	3439	223	869	S654	2739	223	919	S604	2039	223	969	S554	1339	223
820	S703	3425	97	870	S653	2725	97	920	S603	2025	97	970	S553	1325	97
821	S702	3411	223	871	S652	2711	223	921	S602	2011	223	971	S552	1311	223
822	S701	3397	97	872	S651	2697	97	922	S601	1997	97	972	S551	1297	97
823	S700	3383	223	873	S650	2683	223	923	S600	1983	223	973	S550	1283	223
824	S699	3369	97	874	S649	2669	97	924	S599	1969	97	974	S549	1269	97
825	S698	3355	223	875	S648	2655	223	925	S598	1955	223	975	S548	1255	223
826	S697	3341	97	876	S647	2641	97	926	S597	1941	97	976	S547	1241	97
827	S696	3327	223	877	S646	2627	223	927	S596	1927	223	977	S546	1227	223
828	S695	3313	97	878	S645	2613	97	928	S595	1913	97	978	S545	1213	97
829	S694	3299	223	879	S644	2599	223	929	S594	1899	223	979	S544	1199	223
830	S693	3285	97	880	S643	2585	97	930	S593	1885	97	980	S543	1185	97
831	S692	3271	223	881	S642	2571	223	931	S592	1871	223	981	S542	1171	223
832	S691	3257	97	882	S641	2557	97	932	S591	1857	97	982	S541	1157	97
833	S690	3243	223	883	S640	2543	223	933	S590	1843	223	983	S540	1143	223
834	S689	3229	97	884	S639	2529	97	934	S589	1829	97	984	S539	1129	97
835	S688	3215	223	885	S638	2515	223	935	S588	1815	223	985	S538	1115	223
836	S687	3201	97	886	S637	2501	97	936	S587	1801	97	986	S537	1101	97
837	S686	3187	223	887	S636	2487	223	937	S586	1787	223	987	S536	1087	223
838	S685	3173	97	888	S635	2473	97	938	S585	1773	97	988	S535	1073	97
839	S684	3159	223	889	S634	2459	223	939	S584	1759	223	989	S534	1059	223
840	S683	3145	97	890	S633	2445	97	940	S583	1745	97	990	S533	1045	97
841	S682	3131	223	891	S632	2431	223	941	S582	1731	223	991	S532	1031	223
842	S681	3117	97	892	S631	2417	97	942	S581	1717	97	992	S531	1017	97
843	S680	3103	223	893	S630	2403	223	943	S580	1703	223	993	S530	1003	223
844	S679	3089	97	894	S629	2389	97	944	S579	1689	97	994	S529	989	97
845	S678	3075	223	895	S628	2375	223	945	S578	1675	223	995	S528	975	223
846	S677	3061	97	896	S627	2361	97	946	S577	1661	97	996	S527	961	97
847	S676	3047	223	897	S626	2347	223	947	S576	1647	223	997	S526	947	223
848	S675	3033	97	898	S625	2333	97	948	S575	1633	97	998	S525	933	97
849	S674	3019	223	899	S624	2319	223	949	S574	1619	223	999	S524	919	223
850	S673	3005	97	900	S623	2305	97	950	S573	1605	97	1000	S523	905	97

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1001	S522	891	223	1051	DUMMY	107	223	1101	S446	-793	97	1151	S396	-1493	97
1002	S521	877	97	1052	DUMMY	79	223	1102	S445	-807	223	1152	S395	-1507	223
1003	S520	863	223	1053	DUMMY	51	223	1103	S444	-821	97	1153	S394	-1521	97
1004	S519	849	97	1054	DUMMY	23	223	1104	S443	-835	223	1154	S393	-1535	223
1005	S518	835	223	1055	DUMMY	-23	223	1105	S442	-849	97	1155	S392	-1549	97
1006	S517	821	97	1056	DUMMY	-51	223	1106	S441	-863	223	1156	S391	-1563	223
1007	S516	807	223	1057	DUMMY	-79	223	1107	S440	-877	97	1157	S390	-1577	97
1008	S515	793	97	1058	DUMMY	-107	223	1108	S439	-891	223	1158	S389	-1591	223
1009	S514	779	223	1059	DUMMY	-135	223	1109	S438	-905	97	1159	S388	-1605	97
1010	S513	765	97	1060	DUMMY	-163	223	1110	S437	-919	223	1160	S387	-1619	223
1011	S512	751	223	1061	DUMMY	-191	223	1111	S436	-933	97	1161	S386	-1633	97
1012	S511	737	97	1062	DUMMY	-219	223	1112	S435	-947	223	1162	S385	-1647	223
1013	S510	723	223	1063	DUMMY	-247	223	1113	S434	-961	97	1163	S384	-1661	97
1014	S509	709	97	1064	DUMMY	-275	223	1114	S433	-975	223	1164	S383	-1675	223
1015	S508	695	223	1065	DUMMY	-289	97	1115	S432	-989	97	1165	S382	-1689	97
1016	S507	681	97	1066	DUMMY	-303	223	1116	S431	-1003	223	1166	S381	-1703	223
1017	S506	667	223	1067	S480	-317	97	1117	S430	-1017	97	1167	S380	-1717	97
1018	S505	653	97	1068	S479	-331	223	1118	S429	-1031	223	1168	S379	-1731	223
1019	S504	639	223	1069	S478	-345	97	1119	S428	-1045	97	1169	S378	-1745	97
1020	S503	625	97	1070	S477	-359	223	1120	S427	-1059	223	1170	S377	-1759	223
1021	S502	611	223	1071	S476	-373	97	1121	S426	-1073	97	1171	S376	-1773	97
1022	S501	597	97	1072	S475	-387	223	1122	S425	-1087	223	1172	S375	-1787	223
1023	S500	583	223	1073	S474	-401	97	1123	S424	-1101	97	1173	S374	-1801	97
1024	S499	569	97	1074	S473	-415	223	1124	S423	-1115	223	1174	S373	-1815	223
1025	S498	555	223	1075	S472	-429	97	1125	S422	-1129	97	1175	S372	-1829	97
1026	S497	541	97	1076	S471	-443	223	1126	S421	-1143	223	1176	S371	-1843	223
1027	S496	527	223	1077	S470	-457	97	1127	S420	-1157	97	1177	S370	-1857	97
1028	S495	513	97	1078	S469	-471	223	1128	S419	-1171	223	1178	S369	-1871	223
1029	S494	499	223	1079	S468	-485	97	1129	S418	-1185	97	1179	S368	-1885	97
1030	S493	485	97	1080	S467	-499	223	1130	S417	-1199	223	1180	S367	-1899	223
1031	S492	471	223	1081	S466	-513	97	1131	S416	-1213	97	1181	S366	-1913	97
1032	S491	457	97	1082	S465	-527	223	1132	S415	-1227	223	1182	S365	-1927	223
1033	S490	443	223	1083	S464	-541	97	1133	S414	-1241	97	1183	S364	-1941	97
1034	S489	429	97	1084	S463	-555	223	1134	S413	-1255	223	1184	S363	-1955	223
1035	S488	415	223	1085	S462	-569	97	1135	S412	-1269	97	1185	S362	-1969	97
1036	S487	401	97	1086	S461	-583	223	1136	S411	-1283	223	1186	S361	-1983	223
1037	S486	387	223	1087	S460	-597	97	1137	S410	-1297	97	1187	S360	-1997	97
1038	S485	373	97	1088	S459	-611	223	1138	S409	-1311	223	1188	S359	-2011	223
1039	S484	359	223	1089	S458	-625	97	1139	S408	-1325	97	1189	S358	-2025	97
1040	S483	345	97	1090	S457	-639	223	1140	S407	-1339	223	1190	S357	-2039	223
1041	S482	331	223	1091	S456	-653	97	1141	S406	-1353	97	1191	S356	-2053	97
1042	S481	317	97	1092	S455	-667	223	1142	S405	-1367	223	1192	S355	-2067	223
1043	DUMMY	303	223	1093	S454	-681	97	1143	S404	-1381	97	1193	S354	-2081	97
1044	DUMMY	289	97	1094	S453	-695	223	1144	S403	-1395	223	1194	S353	-2095	223
1045	DUMMY	275	223	1095	S452	-709	97	1145	S402	-1409	97	1195	S352	-2109	97
1046	DUMMY	247	223	1096	S451	-723	223	1146	S401	-1423	223	1196	S351	-2123	223
1047	DUMMY	219	223	1097	S450	-737	97	1147	S400	-1437	97	1197	S350	-2137	97
1048	DUMMY	191	223	1098	S449	-751	223	1148	S399	-1451	223	1198	S349	-2151	223
1049	DUMMY	163	223	1099	S448	-765	97	1149	S398	-1465	97	1199	S348	-2165	97
1050	DUMMY	135	223	1100	S447	-779	223	1150	S397	-1479	223	1200	S347	-2179	223

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1201	S346	-2193	97	1251	S296	-2893	97	1301	S246	-3593	97	1351	S196	-4293	97
1202	S345	-2207	223	1252	S295	-2907	223	1302	S245	-3607	223	1352	S195	-4307	223
1203	S344	-2221	97	1253	S294	-2921	97	1303	S244	-3621	97	1353	S194	-4321	97
1204	S343	-2235	223	1254	S293	-2935	223	1304	S243	-3635	223	1354	S193	-4335	223
1205	S342	-2249	97	1255	S292	-2949	97	1305	S242	-3649	97	1355	S192	-4349	97
1206	S341	-2263	223	1256	S291	-2963	223	1306	S241	-3663	223	1356	S191	-4363	223
1207	S340	-2277	97	1257	S290	-2977	97	1307	S240	-3677	97	1357	S190	-4377	97
1208	S339	-2291	223	1258	S289	-2991	223	1308	S239	-3691	223	1358	S189	-4391	223
1209	S338	-2305	97	1259	S288	-3005	97	1309	S238	-3705	97	1359	S188	-4405	97
1210	S337	-2319	223	1260	S287	-3019	223	1310	S237	-3719	223	1360	S187	-4419	223
1211	S336	-2333	97	1261	S286	-3033	97	1311	S236	-3733	97	1361	S186	-4433	97
1212	S335	-2347	223	1262	S285	-3047	223	1312	S235	-3747	223	1362	S185	-4447	223
1213	S334	-2361	97	1263	S284	-3061	97	1313	S234	-3761	97	1363	S184	-4461	97
1214	S333	-2375	223	1264	S283	-3075	223	1314	S233	-3775	223	1364	S183	-4475	223
1215	S332	-2389	97	1265	S282	-3089	97	1315	S232	-3789	97	1365	S182	-4489	97
1216	S331	-2403	223	1266	S281	-3103	223	1316	S231	-3803	223	1366	S181	-4503	223
1217	S330	-2417	97	1267	S280	-3117	97	1317	S230	-3817	97	1367	S180	-4517	97
1218	S329	-2431	223	1268	S279	-3131	223	1318	S229	-3831	223	1368	S179	-4531	223
1219	S328	-2445	97	1269	S278	-3145	97	1319	S228	-3845	97	1369	S178	-4545	97
1220	S327	-2459	223	1270	S277	-3159	223	1320	S227	-3859	223	1370	S177	-4559	223
1221	S326	-2473	97	1271	S276	-3173	97	1321	S226	-3873	97	1371	S176	-4573	97
1222	S325	-2487	223	1272	S275	-3187	223	1322	S225	-3887	223	1372	S175	-4587	223
1223	S324	-2501	97	1273	S274	-3201	97	1323	S224	-3901	97	1373	S174	-4601	97
1224	S323	-2515	223	1274	S273	-3215	223	1324	S223	-3915	223	1374	S173	-4615	223
1225	S322	-2529	97	1275	S272	-3229	97	1325	S222	-3929	97	1375	S172	-4629	97
1226	S321	-2543	223	1276	S271	-3243	223	1326	S221	-3943	223	1376	S171	-4643	223
1227	S320	-2557	97	1277	S270	-3257	97	1327	S220	-3957	97	1377	S170	-4657	97
1228	S319	-2571	223	1278	S269	-3271	223	1328	S219	-3971	223	1378	S169	-4671	223
1229	S318	-2585	97	1279	S268	-3285	97	1329	S218	-3985	97	1379	S168	-4685	97
1230	S317	-2599	223	1280	S267	-3299	223	1330	S217	-3999	223	1380	S167	-4699	223
1231	S316	-2613	97	1281	S266	-3313	97	1331	S216	-4013	97	1381	S166	-4713	97
1232	S315	-2627	223	1282	S265	-3327	223	1332	S215	-4027	223	1382	S165	-4727	223
1233	S314	-2641	97	1283	S264	-3341	97	1333	S214	-4041	97	1383	S164	-4741	97
1234	S313	-2655	223	1284	S263	-3355	223	1334	S213	-4055	223	1384	S163	-4755	223
1235	S312	-2669	97	1285	S262	-3369	97	1335	S212	-4069	97	1385	S162	-4769	97
1236	S311	-2683	223	1286	S261	-3383	223	1336	S211	-4083	223	1386	S161	-4783	223
1237	S310	-2697	97	1287	S260	-3397	97	1337	S210	-4097	97	1387	S160	-4797	97
1238	S309	-2711	223	1288	S259	-3411	223	1338	S209	-4111	223	1388	S159	-4811	223
1239	S308	-2725	97	1289	S258	-3425	97	1339	S208	-4125	97	1389	S158	-4825	97
1240	S307	-2739	223	1290	S257	-3439	223	1340	S207	-4139	223	1390	S157	-4839	223
1241	S306	-2753	97	1291	S256	-3453	97	1341	S206	-4153	97	1391	S156	-4853	97
1242	S305	-2767	223	1292	S255	-3467	223	1342	S205	-4167	223	1392	S155	-4867	223
1243	S304	-2781	97	1293	S254	-3481	97	1343	S204	-4181	97	1393	S154	-4881	97
1244	S303	-2795	223	1294	S253	-3495	223	1344	S203	-4195	223	1394	S153	-4895	223
1245	S302	-2809	97	1295	S252	-3509	97	1345	S202	-4209	97	1395	S152	-4909	97
1246	S301	-2823	223	1296	S251	-3523	223	1346	S201	-4223	223	1396	S151	-4923	223
1247	S300	-2837	97	1297	S250	-3537	97	1347	S200	-4237	97	1397	S150	-4937	97
1248	S299	-2851	223	1298	S249	-3551	223	1348	S199	-4251	223	1398	S149	-4951	223
1249	S298	-2865	97	1299	S248	-3565	97	1349	S198	-4265	97	1399	S148	-4965	97
1250	S297	-2879	223	1300	S247	-3579	223	1350	S197	-4279	223	1400	S147	-4979	223

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1401	S146	-4993	97	1451	S96	-5693	97	1501	S46	-6393	97	1551	G1	-7099	97
1402	S145	-5007	223	1452	S95	-5707	223	1502	S45	-6407	223	1552	G3	-7115	223
1403	S144	-5021	97	1453	S94	-5721	97	1503	S44	-6421	97	1553	G5	-7131	97
1404	S143	-5035	223	1454	S93	-5735	223	1504	S43	-6435	223	1554	G7	-7147	223
1405	S142	-5049	97	1455	S92	-5749	97	1505	S42	-6449	97	1555	G9	-7163	97
1406	S141	-5063	223	1456	S91	-5763	223	1506	S41	-6463	223	1556	G11	-7179	223
1407	S140	-5077	97	1457	S90	-5777	97	1507	S40	-6477	97	1557	G13	-7195	97
1408	S139	-5091	223	1458	S89	-5791	223	1508	S39	-6491	223	1558	G15	-7211	223
1409	S138	-5105	97	1459	S88	-5805	97	1509	S38	-6505	97	1559	G17	-7227	97
1410	S137	-5119	223	1460	S87	-5819	223	1510	S37	-6519	223	1560	G19	-7243	223
1411	S136	-5133	97	1461	S86	-5833	97	1511	S36	-6533	97	1561	G21	-7259	97
1412	S135	-5147	223	1462	S85	-5847	223	1512	S35	-6547	223	1562	G23	-7275	223
1413	S134	-5161	97	1463	S84	-5861	97	1513	S34	-6561	97	1563	G25	-7291	97
1414	S133	-5175	223	1464	S83	-5875	223	1514	S33	-6575	223	1564	G27	-7307	223
1415	S132	-5189	97	1465	S82	-5889	97	1515	S32	-6589	97	1565	G29	-7323	97
1416	S131	-5203	223	1466	S81	-5903	223	1516	S31	-6603	223	1566	G31	-7339	223
1417	S130	-5217	97	1467	S80	-5917	97	1517	S30	-6617	97	1567	G33	-7355	97
1418	S129	-5231	223	1468	S79	-5931	223	1518	S29	-6631	223	1568	G35	-7371	223
1419	S128	-5245	97	1469	S78	-5945	97	1519	S28	-6645	97	1669	G37	-7387	97
1420	S127	-5259	223	1470	S77	-5959	223	1520	S27	-6659	223	1570	G39	-7403	223
1421	S126	-5273	97	1471	S76	-5973	97	1521	S26	-6673	97	1571	G41	-7419	97
1422	S125	-5287	223	1472	S75	-5987	223	1522	S25	-6687	223	1572	G43	-7435	223
1423	S124	-5301	97	1473	S74	-6001	97	1523	S24	-6701	97	1573	G45	-7451	97
1424	S123	-5315	223	1474	S73	-6015	223	1524	S23	-6715	223	1574	G47	-7467	223
1425	S122	-5329	97	1475	S72	-6029	97	1525	S22	-6729	97	1575	G49	-7483	97
1426	S121	-5343	223	1476	S71	-6043	223	1526	S21	-6743	223	1576	G51	-7499	223
1427	S120	-5357	97	1477	S70	-6057	97	1527	S20	-6757	97	1577	G53	-7515	97
1428	S119	-5371	223	1478	S69	-6071	223	1528	S19	-6771	223	1578	G55	-7531	223
1429	S118	-5385	97	1479	S68	-6085	97	1529	S18	-6785	97	1579	G57	-7547	97
1430	S117	-5399	223	1480	S67	-6099	223	1530	S17	-6799	223	1580	G59	-7563	223
1431	S116	-5413	97	1481	S66	-6113	97	1531	S16	-6813	97	1581	G61	-7579	97
1432	S115	-5427	223	1482	S65	-6127	223	1532	S15	-6827	223	1582	G63	-7595	223
1433	S114	-5441	97	1483	S64	-6141	97	1533	S14	-6841	97	1583	G65	-7611	97
1434	S113	-5455	223	1484	S63	-6155	223	1534	S13	-6855	223	1584	G67	-7627	223
1435	S112	-5469	97	1485	S62	-6169	97	1535	S12	-6869	97	1585	G69	-7643	97
1436	S111	-5483	223	1486	S61	-6183	223	1536	S11	-6883	223	1586	G71	-7659	223
1437	S110	-5497	97	1487	S60	-6197	97	1537	S10	-6897	97	1587	G73	-7675	97
1438	S109	-5511	223	1488	S59	-6211	223	1538	S9	-6911	223	1588	G75	-7691	223
1439	S108	-5525	97	1489	S58	-6225	97	1539	S8	-6925	97	1589	G77	-7707	97
1440	S107	-5539	223	1490	S57	-6239	223	1540	S7	-6939	223	1590	G79	-7723	223
1441	S106	-5553	97	1491	S56	-6253	97	1541	S6	-6953	97	1591	G81	-7739	97
1442	S105	-5567	223	1492	S55	-6267	223	1542	S5	-6967	223	1592	G83	-7755	223
1443	S104	-5581	97	1493	S54	-6281	97	1543	S4	-6981	97	1593	G85	-7771	97
1444	S103	-5595	223	1494	S53	-6295	223	1544	S3	-6995	223	1594	G87	-7787	223
1445	S102	-5609	97	1495	S52	-6309	97	1545	S2	-7009	97	1595	G89	-7803	97
1446	S101	-5623	223	1496	S51	-6323	223	1546	S1	-7023	223	1596	G91	-7819	223
1447	S100	-5637	97	1497	S50	-6337	97	1547	DUMMY	-7037	97	1597	G93	-7835	97
1448	S99	-5651	223	1498	S49	-6351	223	1548	DUMMY	-7051	223	1598	G95	-7851	223
1449	S98	-5665	97	1499	S48	-6365	97	1549	DUMMY	-7067	97	1599	G97	-7867	97
1450	S97	-5679	223	1500	S47	-6379	223	1550	DUMMY	-7083	223	1600	G99	-7883	223

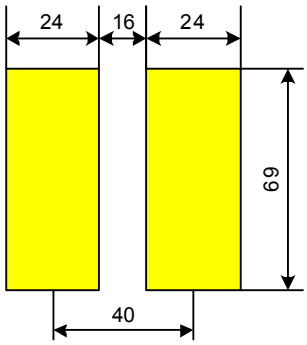
No.	Pad name	X	Y
1601	G101	-7899	97
1602	G103	-7915	223
1603	G105	-7931	97
1604	G107	-7947	223
1605	G109	-7963	97
1606	G111	-7979	223
1607	G113	-7995	97
1608	G115	-8011	223
1609	G117	-8027	97
1610	G119	-8043	223
1611	G121	-8059	97
1612	G123	-8075	223
1613	G125	-8091	97
1614	G127	-8107	223
1615	G129	-8123	97
1616	G131	-8139	223
1617	G133	-8155	97
1618	G135	-8171	223
1619	G137	-8187	97
1620	G139	-8203	223
1621	G141	-8219	97
1622	G143	-8235	223
1623	G145	-8251	97
1624	G147	-8267	223
1625	G149	-8283	97
1626	G151	-8299	223
1627	G153	-8315	97
1628	G155	-8331	223
1629	G157	-8347	97
1630	G159	-8363	223
1631	G161	-8379	97
1632	G163	-8395	223
1633	G165	-8411	97
1634	G167	-8427	223
1635	G169	-8443	97
1636	G171	-8459	223
1637	G173	-8475	97
1638	G175	-8491	223
1639	G177	-8507	97
1640	G179	-8523	223
1641	G181	-8539	97
1642	G183	-8555	223
1643	G185	-8571	97
1644	G187	-8587	223
1645	G189	-8603	97
1646	G191	-8619	223
1647	G193	-8635	97
1648	G195	-8651	223
1649	G197	-8667	97
1650	G199	-8683	223

No.	Pad name	X	Y
1651	G201	-8699	97
1652	G203	-8715	223
1653	G205	-8731	97
1654	G207	-8747	223
1655	G209	-8763	97
1656	G211	-8779	223
1657	G213	-8795	97
1658	G215	-8811	223
1659	G217	-8827	97
1660	G219	-8843	223
1661	G221	-8859	97
1662	G223	-8875	223
1663	G225	-8891	97
1664	G227	-8907	223
1665	G229	-8923	97
1666	G231	-8939	223
1667	G233	-8955	97
1668	G235	-8971	223
1669	G237	-8987	97
1670	G239	-9003	223
1671	DUMMY	-9019	97
1672	DUMMY	-9035	223

Alignment mark	X	Y
A1	-9200	225
A2	9200	225

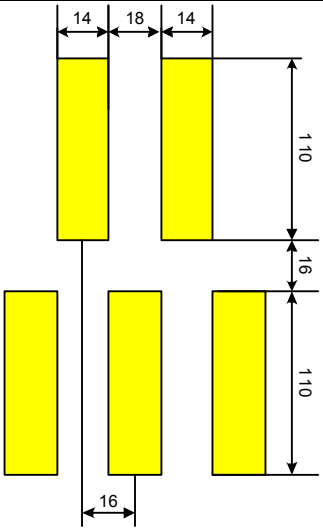
6.1. Bump Arrangement

Input Pad
(No.1 ~ No.436)



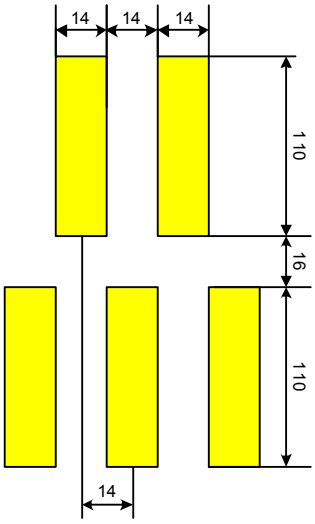
Unit: um

Output Pad
(No.437 ~ No.1672)



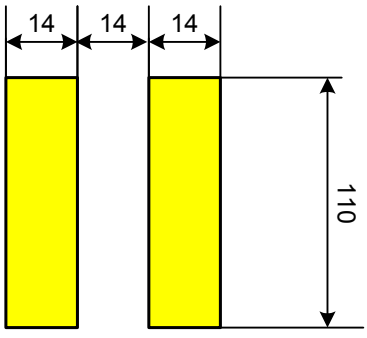
No. 437 ~ No. 561
No.1549 ~ No.1672

Unit: um



No. 562 ~ No.1045
No.1065 ~ No.1548

Unit: um



No.1046 ~ No.1054
No.1055 ~ No.1064

Unit: um

7. Function Description

7.1. MPU interfaces

ILI9342 provides the 8-/9-/16-/18-bit parallel system interface for 8080 series and 6800 series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MPU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MPU-Interface Mode	Pins in use
0	0	0	0	6800 MPU 8-bit bus interface	DB[7:0],R/WX,E,CSX,D/CX
0	0	0	1	6800 MPU 9-bit bus interface	DB[8:0] ,R/WX,E,CSX,D/CX
0	0	1	0	6800 MPU 16-bit bus interface	DB[15:0] ,R/WX,E,CSX,D/CX
0	0	1	1	6800 MPU 18-bit bus interface	DB[17:0] ,R/WX,E,CSX,D/CX
0	1	0	0	8080 MPU 8-bit bus interface	DB[7:0],WRX,RDX,CSX,D/CX
0	1	0	1	8080 MPU 9-bit bus interface	DB[8:0] ,WRX,RDX,CSX,D/CX
0	1	1	0	8080 MPU 16-bit bus interface	DB[15:0] ,WRX,RDX,CSX,D/CX
0	1	1	1	8080 MPU 18-bit bus interface	DB[17:0] ,WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface	SCL,SDA,CSX
1	1	1	1	4-wire 8-bit data serial interface	SCL,SDA,D/CX,CSX

7.1.2. 8080-Series Parallel Interface

ILI9342 can be accessed via 8-/9-/16-/18-bit MPU 8080-series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9342 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and DB[17:0] is parallel data bus.

ILI9342 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the MPU controller and LCD driver chip. The 8080-interface selection is done when IM3 pin is low state (DGND level). Interface bus width can be selected by IM [3:0] bits.

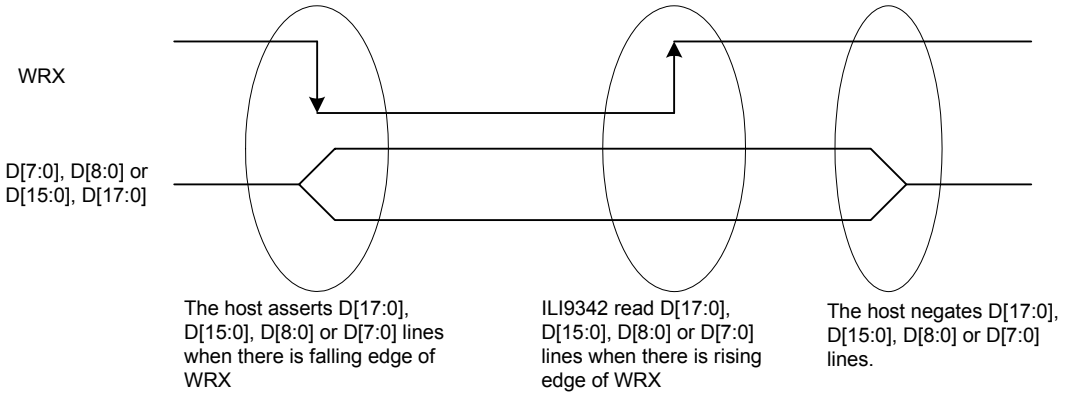
The selection of 8080-series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MPU-Interface Mode	CSX	WRX	RDX	D/CX	Function
0	1	0	0	8080 MPU 8-bit bus interface	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	0	1	8080 MPU 9-bit bus interface	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	0	8080 MPU 16-bit bus interface	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	1	8080 MPU 18-bit bus interface	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

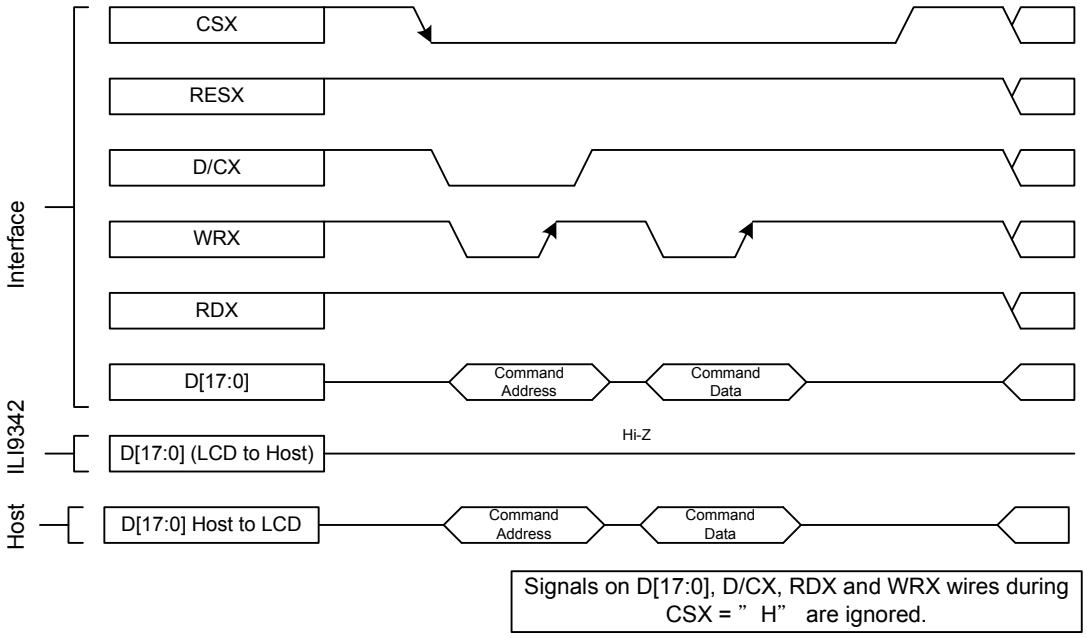
7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080 MPU interface.



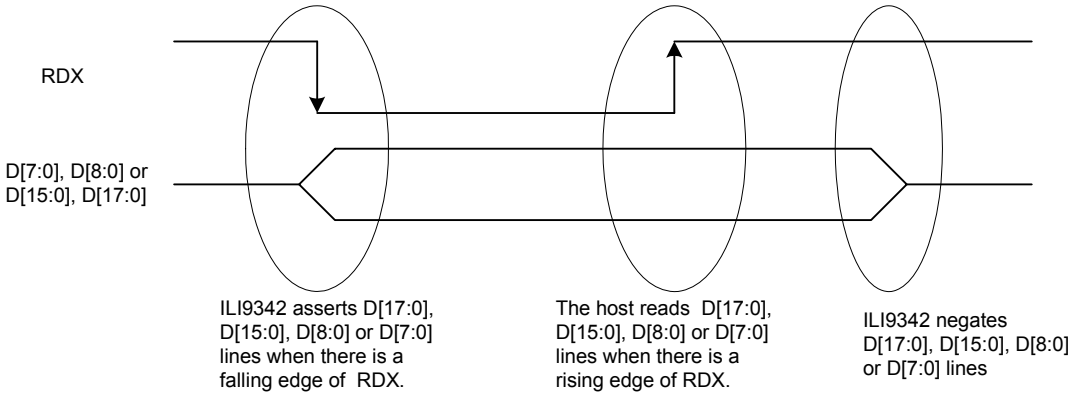
Note: WRX is an unsynchronized signal (It can be stopped)



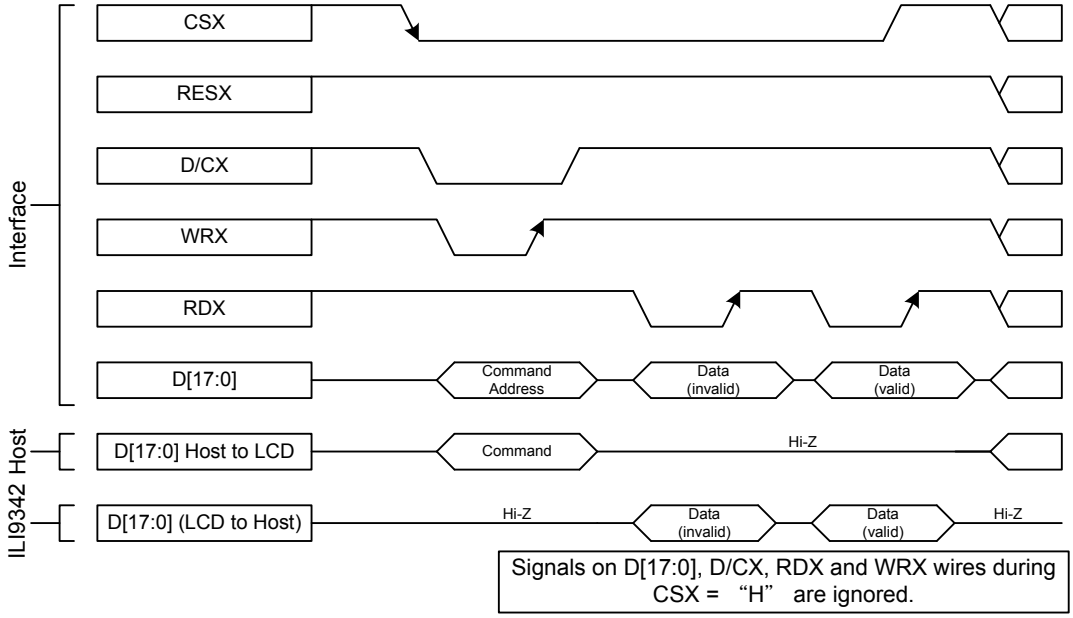
7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080 MPU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.5. 6800-Series Parallel Interface

ILI9342 can be accessed via 8-/9-/16-/18-bit MPU parallel interface with 6800-series. The chip-select CSX (active low) signal is used to enable or disable ILI9342. The RESX (active low) signal is an external reset signal. The E signal is the enable signal of Read/Write operation. The R/WX is the select signal for Read/Write operation and D [17:0] is parallel data.

ILI9342 supports two kinds of interface operation, Fixed E mode and Clocked E mode. In Clocked E mode, host reads the data at the falling edge of E signal when R/WX ='1' and writes the data at the falling of E signal when R/WX ='0'. In Fixed E mode, host reads the data at rising edge of CSX signal when R/WX='1' and writes the data at rising edge of CSX signal when R/WX='0'. The D/CX is a control signal which tells if the information on D [17:0] is a command or a data. When D/CX='1', the information of D [17:0] bits are display RAM data or command parameters. When D/CX='0', the information of DB[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between micro controller host and LCD driver chip. The Interface bus width can be selected by IM [3:0] bits.

MPU 6800-series interface supports two modes: Fixed E and Clocked E. The functions are shown as below:

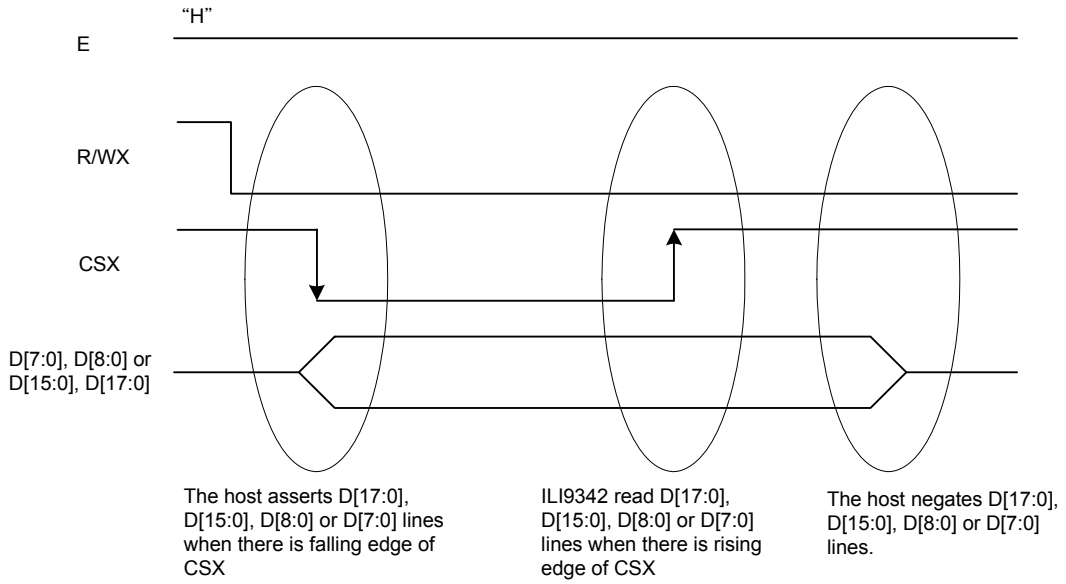
IM3	IM2	IM1	IM0	MPU Interface Mode	CSX	R/WX	E	D/CX	Function
0	0	0	0	6800-series MPU 8-bit interface (Fixed E mode)	↑	"L"	"H"	"L"	Write command code.
					↑	"H"	"H"	"H"	Read internal status.
					↑	"L"	"H"	"H"	Write parameter or display data.
					↑	"H"	"H"	"H"	Reads parameter or display data.
0	0	0	1	6800-series MPU 9-bit interface (Fixed E mode)	↑	"L"	"H"	"L"	Write command code.
					↑	"H"	"H"	"H"	Read internal status.
					↑	"L"	"H"	"H"	Write parameter or display data.
					↑	"H"	"H"	"H"	Reads parameter or display data.
0	0	1	0	6800-series MPU 16-bit interface (Fixed E mode)	↑	"L"	"H"	"L"	Write command code.
					↑	"H"	"H"	"H"	Read internal status.
					↑	"L"	"H"	"H"	Write parameter or display data.
					↑	"H"	"H"	"H"	Reads parameter or display data.
0	0	1	1	6800-series MPU 18-bit interface (Fixed E mode)	↑	"L"	"H"	"L"	Write command code.
					↑	"H"	"H"	"H"	Read internal status.
					↑	"L"	"H"	"H"	Write parameter or display data.
					↑	"H"	"H"	"H"	Reads parameter or display data.

IM3	IM2	IM1	IM0	MPU Interface Mode	CSX	R/WX	E	D/CX	Function
0	0	0	0	6800-series MPU 8-bit interface (Clocked E mode)	"L"	"L"	↓	"L"	Write command code.
					"L"	"H"	↓	"H"	Read internal status.
					"L"	"L"	↓	"H"	Write parameter or display data.
					"L"	"H"	↓	"H"	Reads parameter or display data.
0	0	0	1	6800-series MPU 9-bit interface (Clocked E mode)	"L"	"L"	↓	"L"	Write command code.
					"L"	"H"	↓	"H"	Read internal status.
					"L"	"L"	↓	"H"	Write parameter or display data.
					"L"	"H"	↓	"H"	Reads parameter or display data.
0	0	1	0	6800-series MPU 16-bit interface (Clocked E mode)	"L"	"L"	↓	"L"	Write command code.
					"L"	"H"	↓	"H"	Read internal status.
					"L"	"L"	↓	"H"	Write parameter or display data.
					"L"	"H"	↓	"H"	Reads parameter or display data.
0	0	1	1	6800-series MPU 18-bit interface (Clocked E mode)	"L"	"L"	↓	"L"	Write command code.
					"L"	"H"	↓	"H"	Read internal status.
					"L"	"L"	↓	"H"	Write parameter or display data.
					"L"	"H"	↓	"H"	Reads parameter or display data.

7.1.6. Write Cycle Sequence

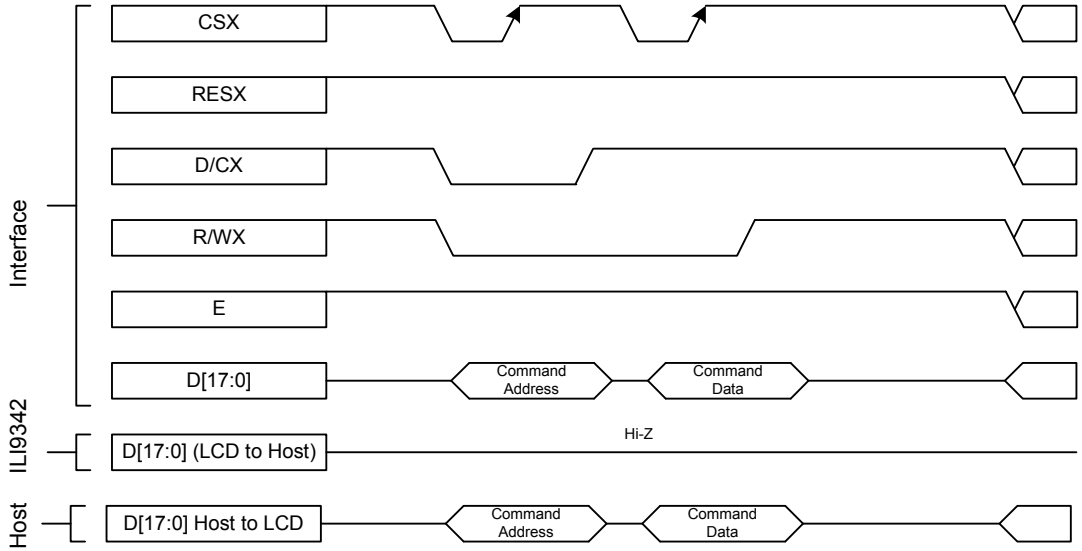
During a write cycle, host writes commands or data to ILI9342 via the interface. The 6800-series MPU interface supports two modes: Fixed E mode and Clocked E mode. Both modes utilize CSX, D/CX, R/WX and E signals as well as all eight (D [7:0]), nine (D [8:0]), sixteen (D [15:0]) and eighteen (D [17:0]) information signals. D/CX is driven to “low” while a command is present on the interface and pulled to “high” when data is on the interface.

Fixed E mode write cycle is described in the figure below.

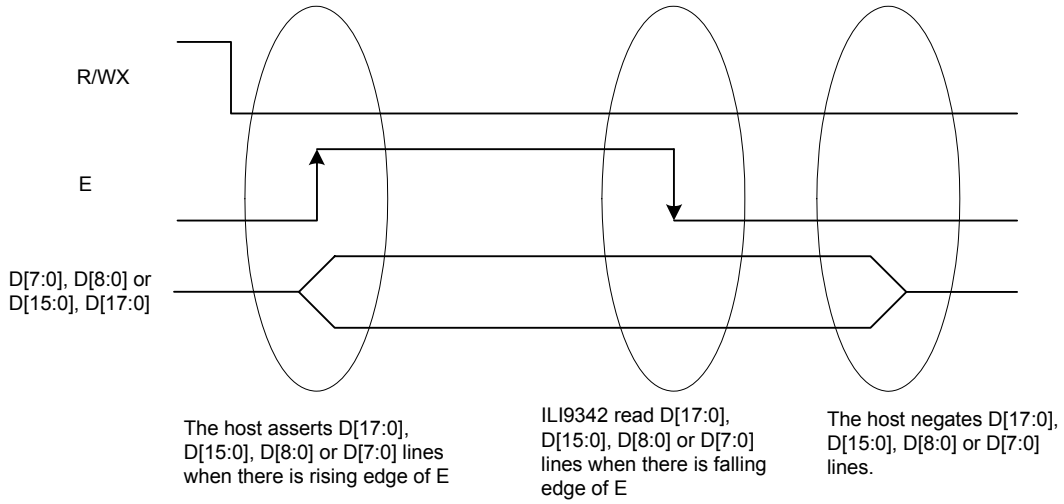


Note: (1) E signal is tied up to “high” in Fixed E mode.

(2) CSX is unsynchronized signal (it can be stopped).

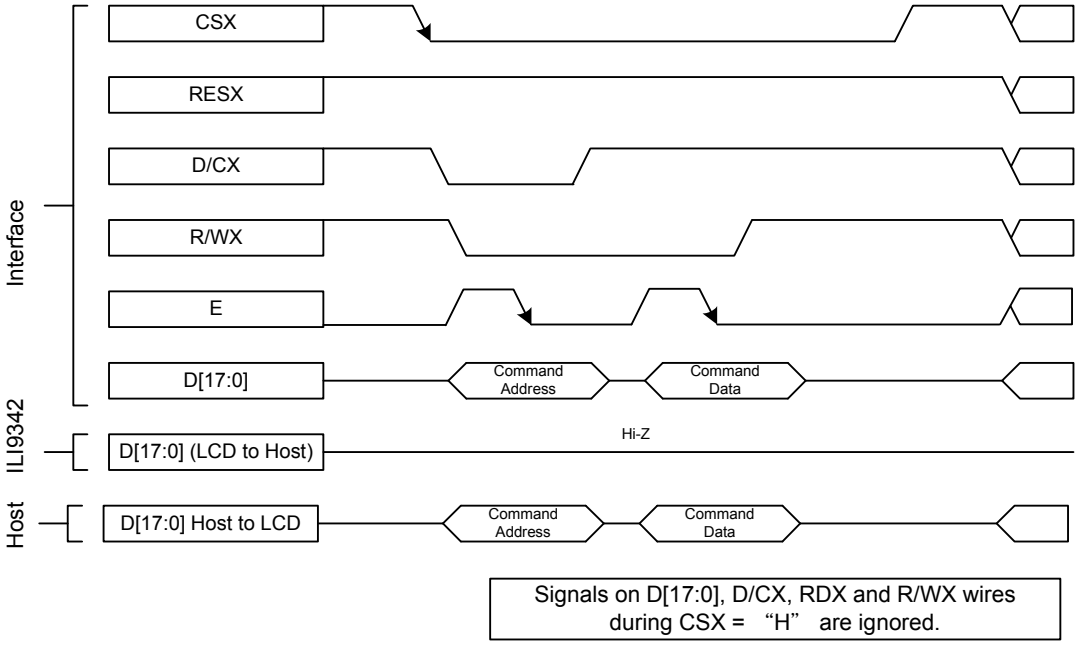


Clocked E mode write cycle is described in the figure below.



Note: (1) E is an unsynchronized signal (It can be stopped).

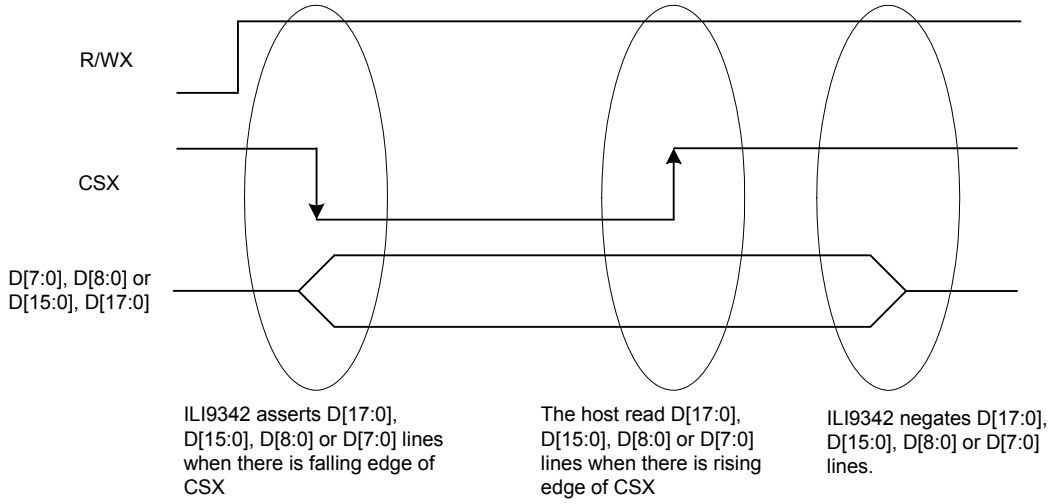
(2) CSX is asserted (taken low) for the same duration as the information signals.

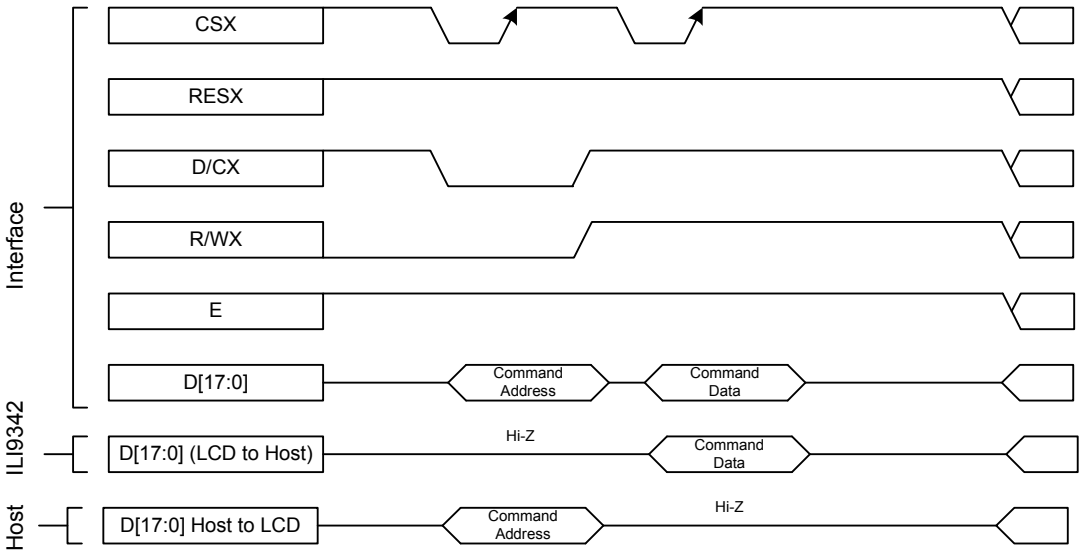


7.1.7. Read Cycle Sequence

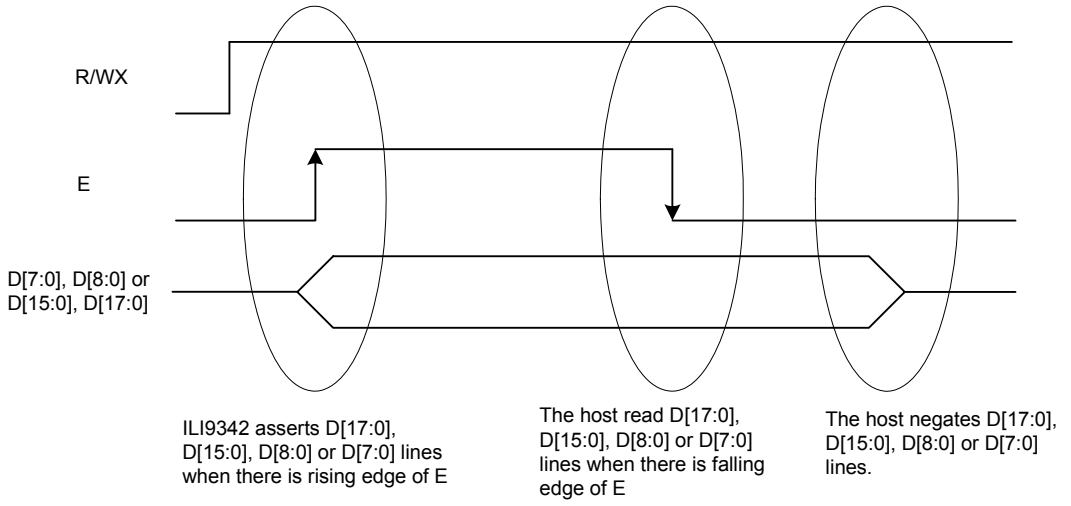
During a read cycle, host processor reads information (command or/and data) from ILI9342 via the interface. The 6800-series MPU interface supports two modes: Fixed E mode and Clocked E mode. Both modes utilize CSX, D/CX, R/WX and E signals as well as all eight (D [7:0]), nine (D [8:0]), sixteen (D [15:0]) and eighteen (D [17:0]) information signals. D/CX is driven to “low” during the entire read cycle.

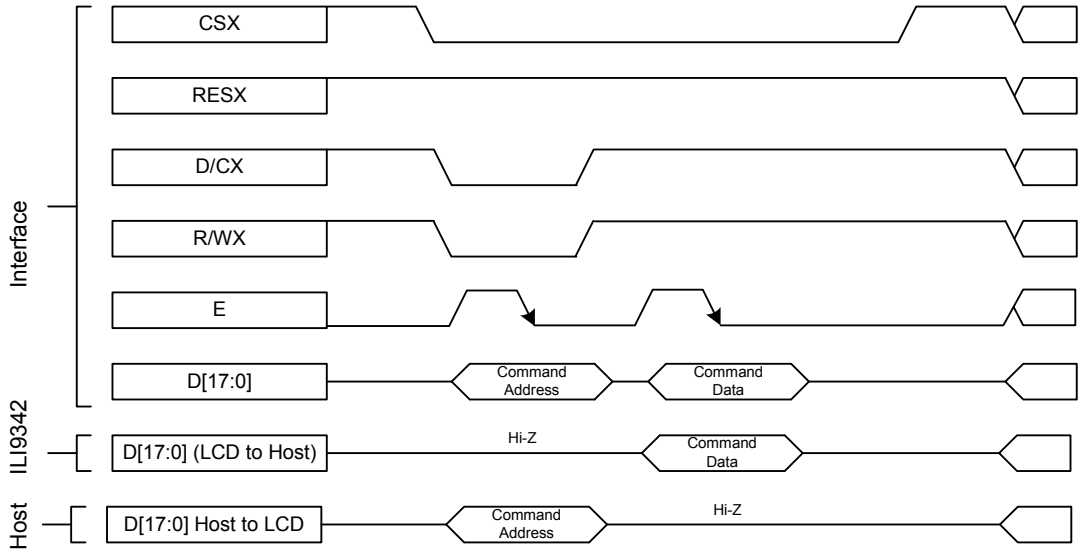
Fixed E mode read cycle is described in the figure below.





Clocked E mode write cycle is described in the figure below.





7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

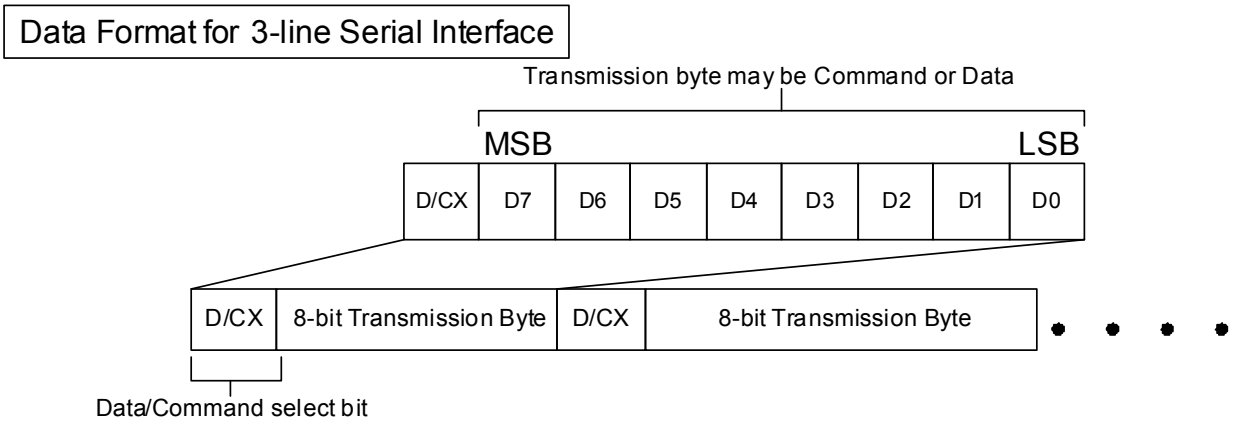
IM3	IM2	IM1	IM0	MPU-Interface Mode	CSX	D/CX	SCL	Function
1	1	0	1	3-line serial interface	"L"	-	↑	Read/Write command, parameter or display data.
1	1	1	1	4-line serial interface	"L"	'H/L"	↑	Read/Write command, parameter or display data.

ILI9342 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9342. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D [17:0]), which are not used, must be connected to DGND. Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

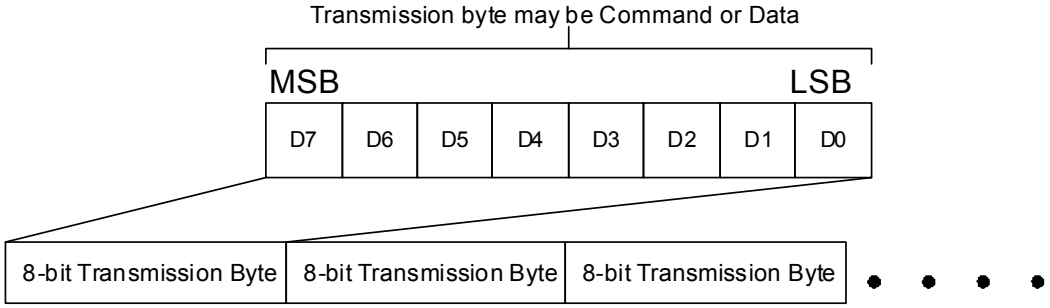
7.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to ILI9342. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to ILI9342 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

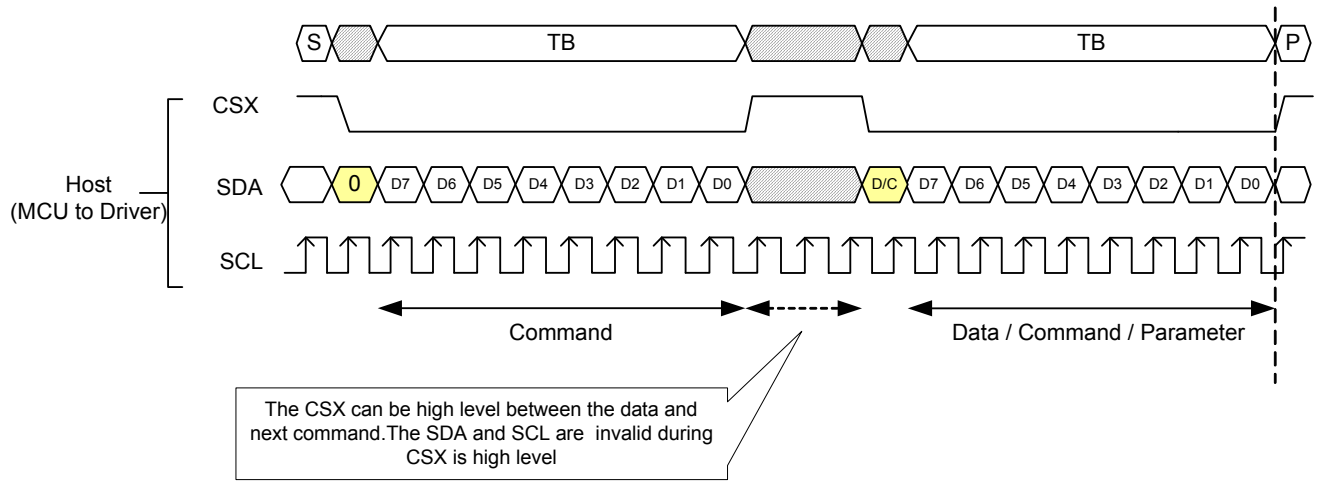


Data Format for 4-line Serial Interface

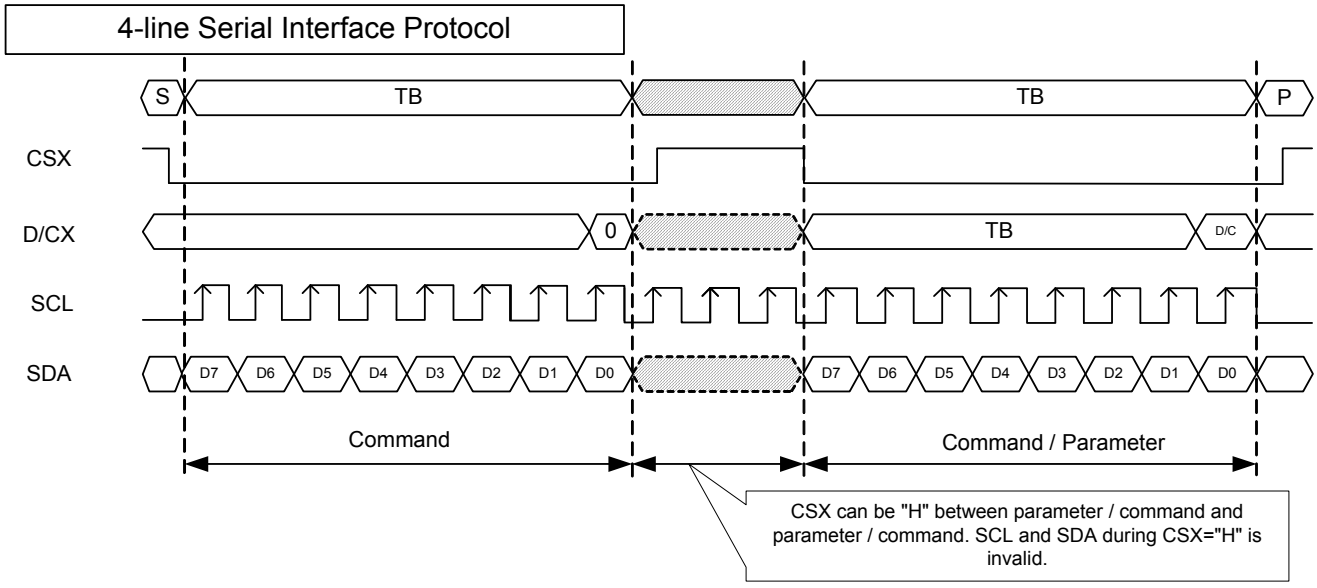


Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9342 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

3-line Serial Interface Protocol



4-line Serial Interface Protocol

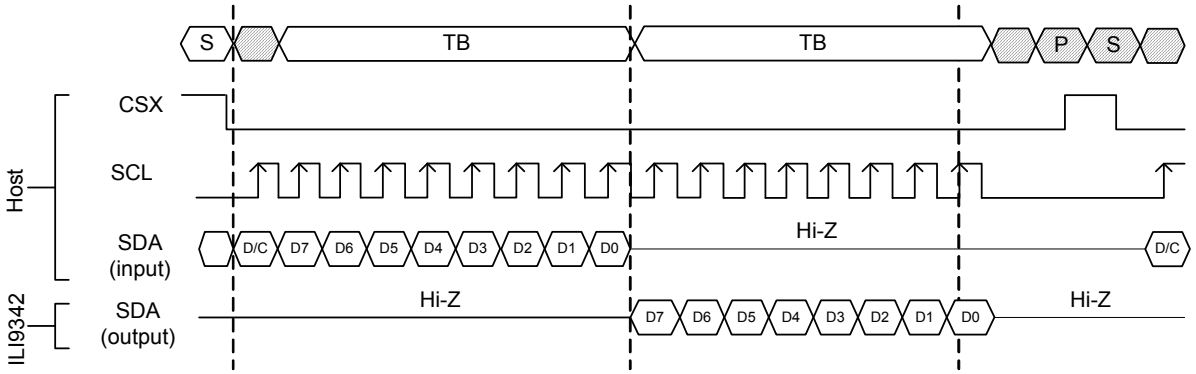


7.1.10. Read Cycle Sequence

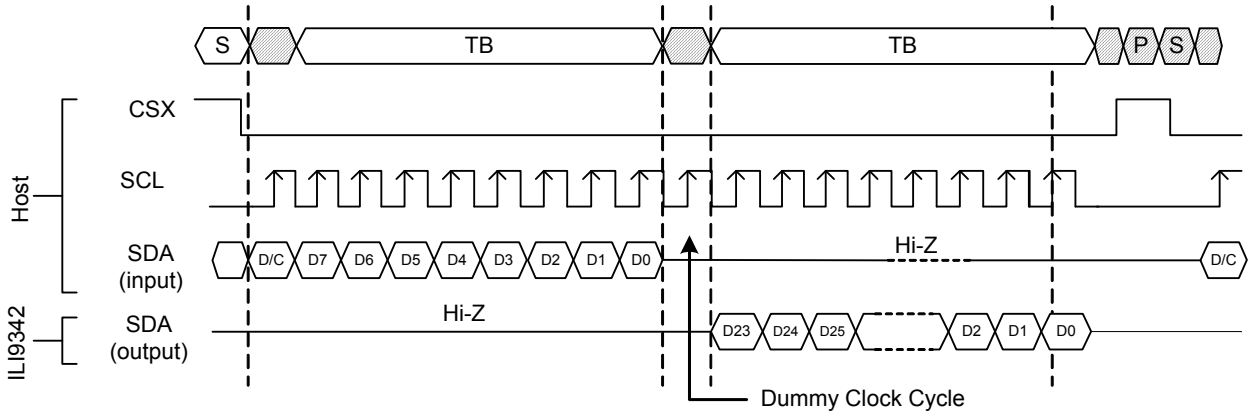
The read mode of interface means that the host reads register's parameter or display data from ILI9342. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9342 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol

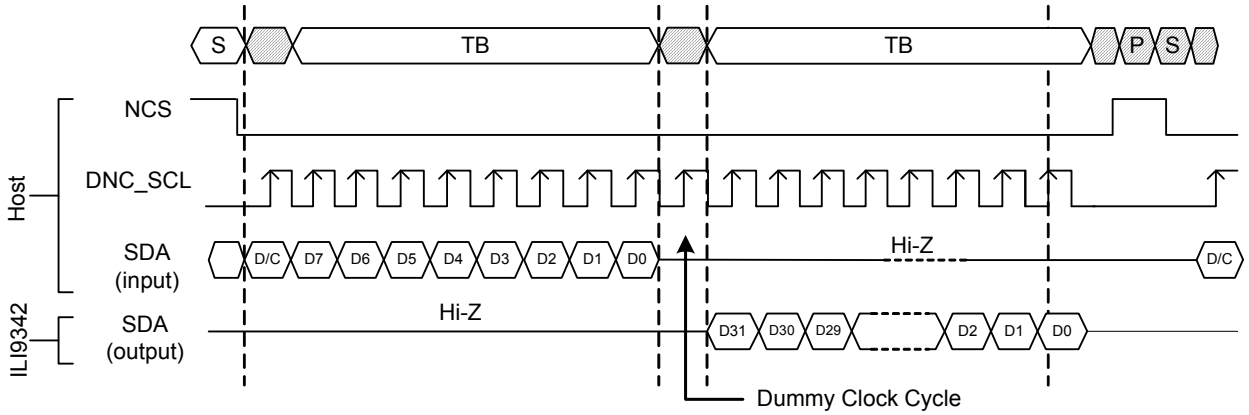
3-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



3-wire Serial Protocol (for RDDID command: 24-bit read)

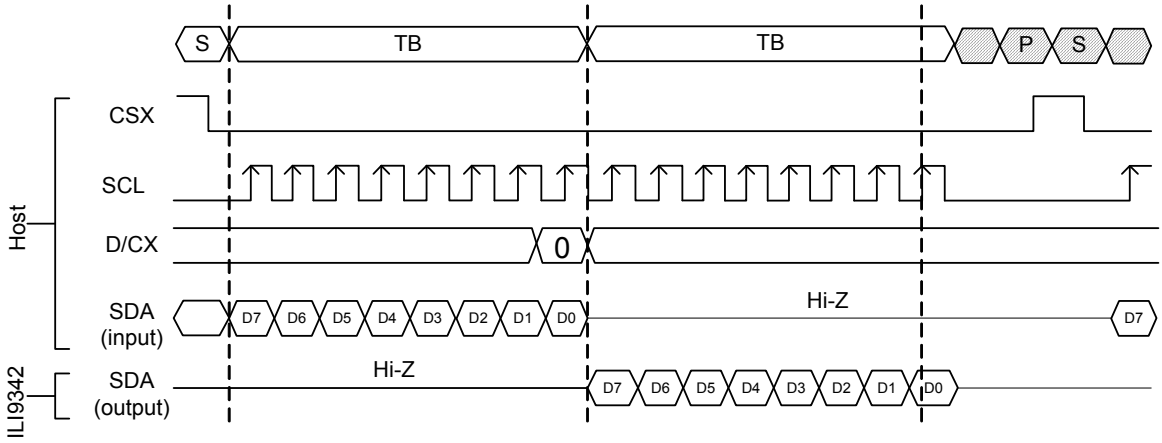


3-wire Serial Protocol (for RDDST command: 32-bit read)

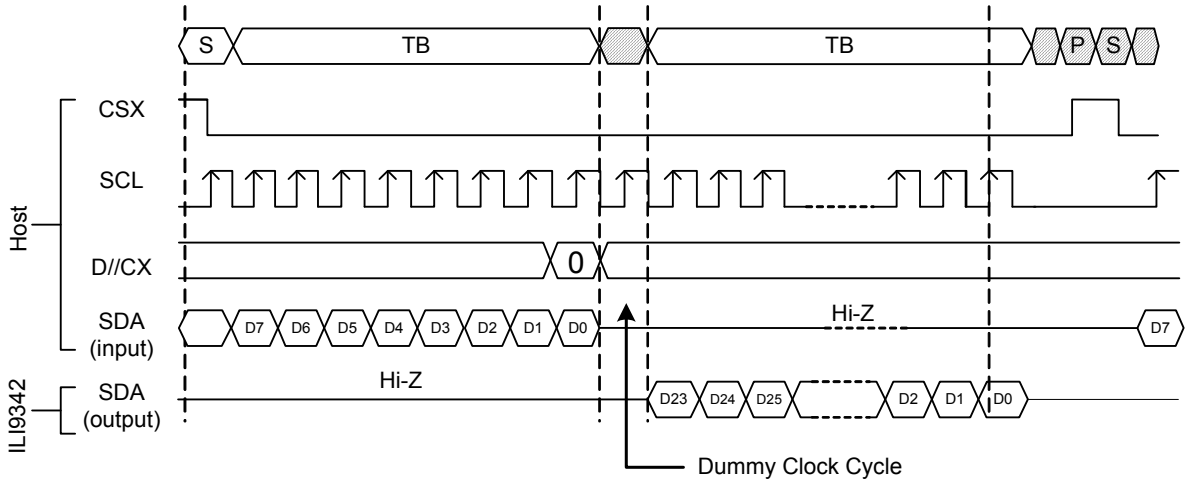


4-wire Serial Interface Protocol

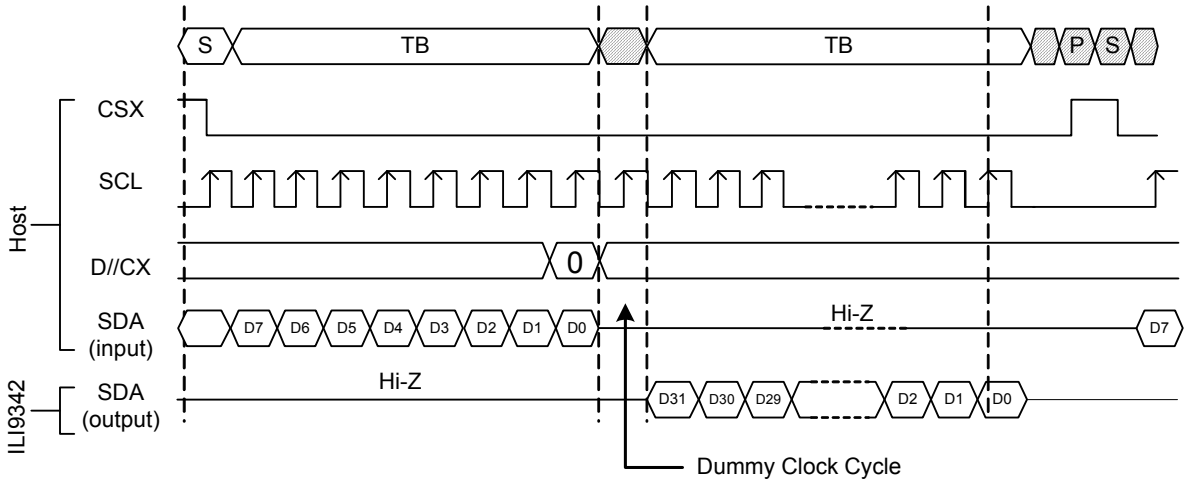
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-line Serial Protocol (for RDDID command: 24-bit read)

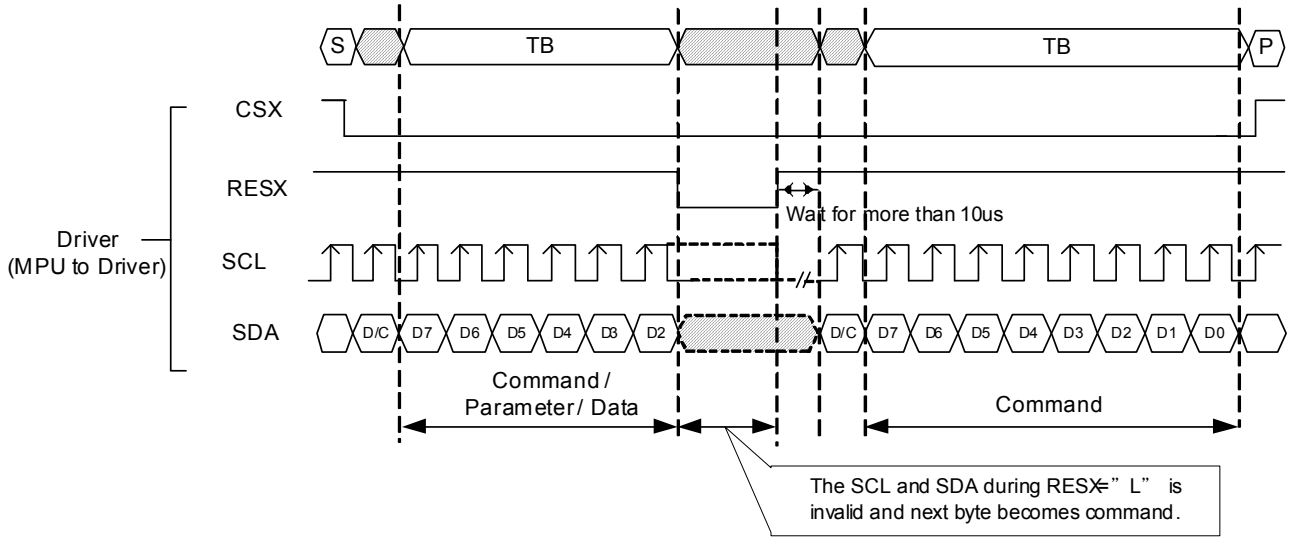


4-line Serial Protocol (for RDDST command: 32-bit read)

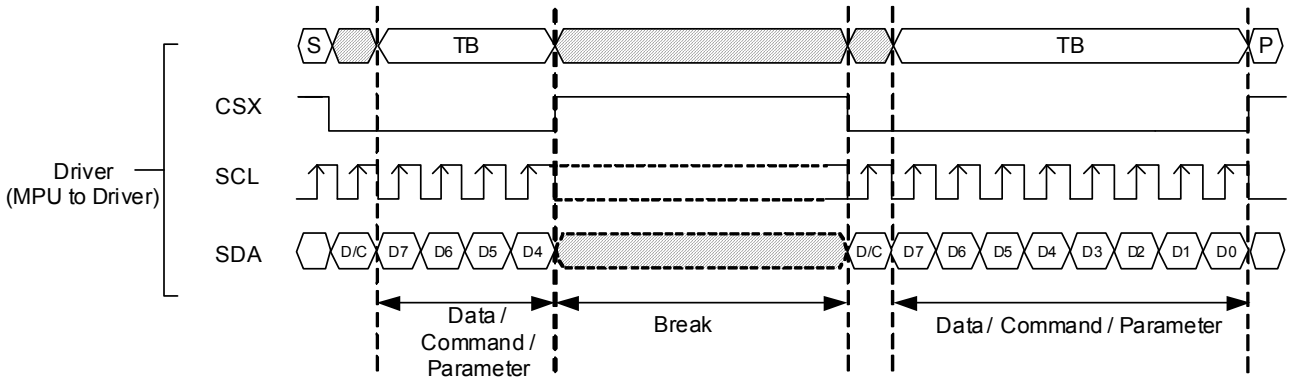


7.1.11. Data Transfer Break and Recovery

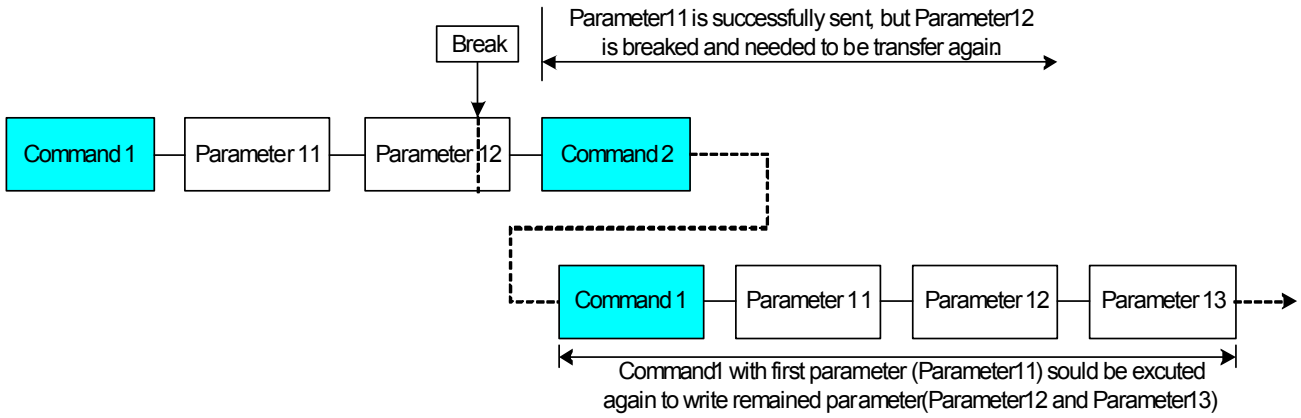
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



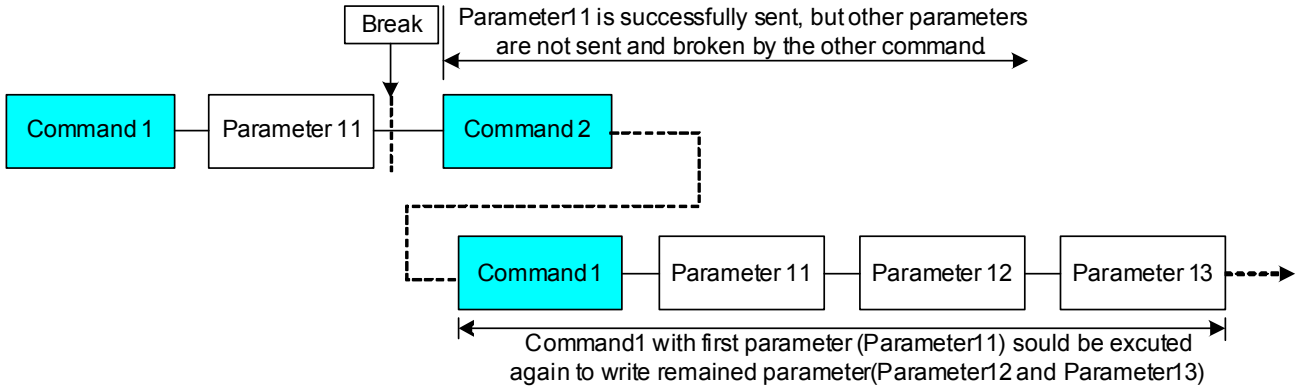
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.



7.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9342 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

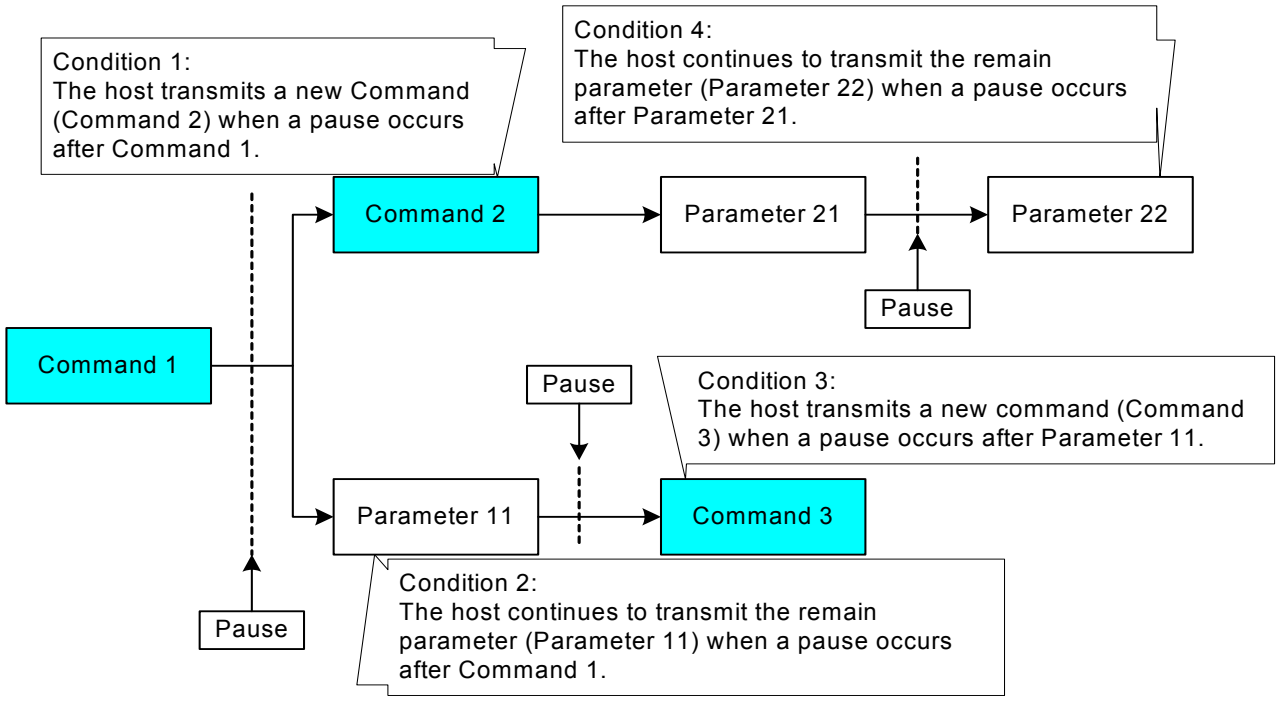
This applies to the following 4 conditions:

1) Command-Pause-Command

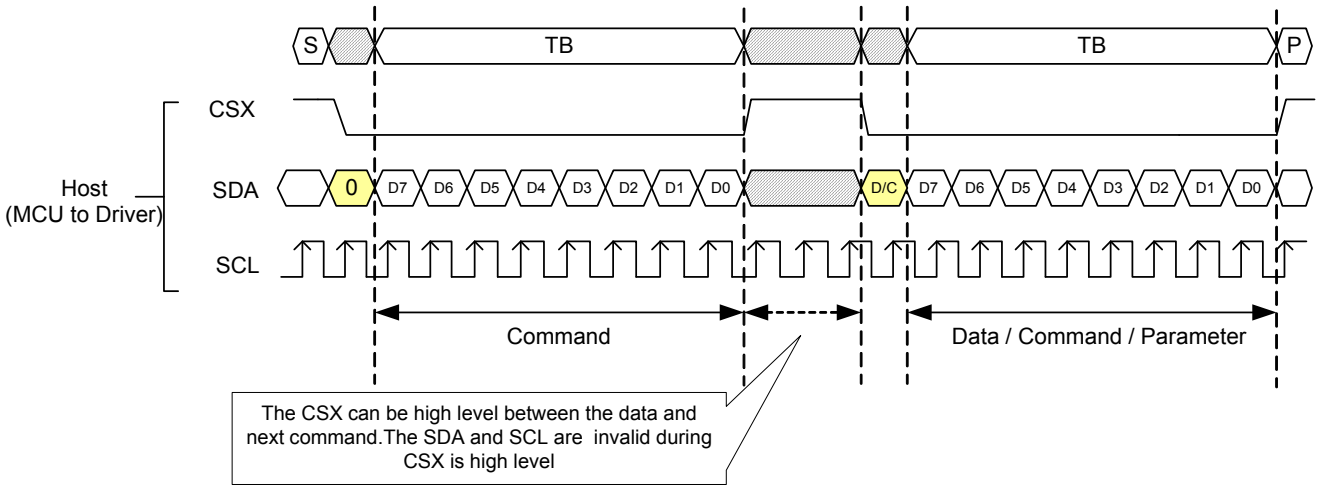
2) Command-Pause-Parameter

3) Parameter-Pause-Command

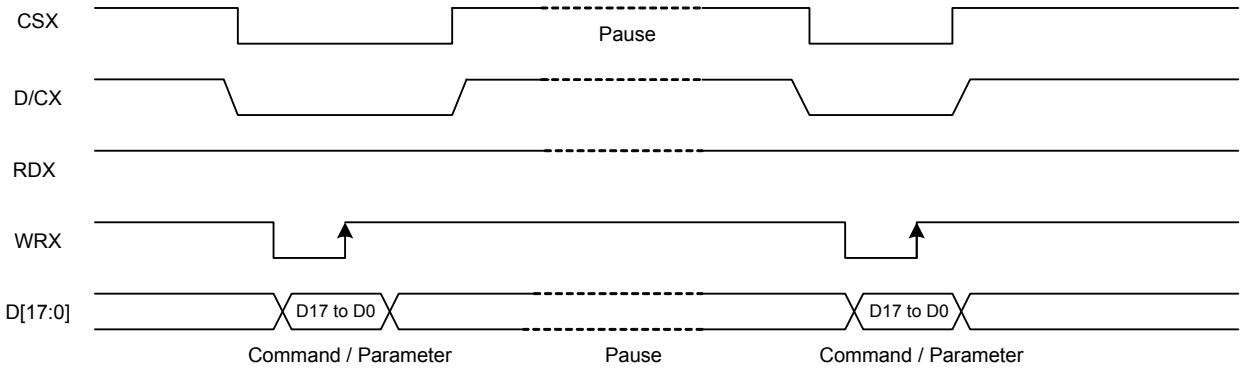
4) Parameter-Pause-Parameter



7.1.13. Serial Interface Pause (3_wire)



7.1.14. Parallel Interface Pause

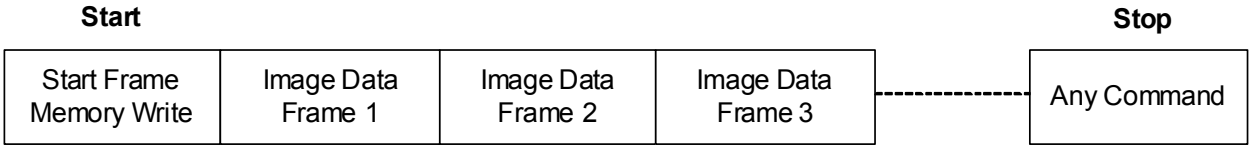


7.1.15. Data Transfer Mode

ILI9342 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

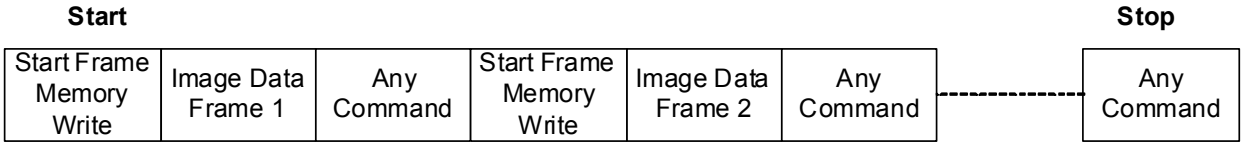
7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9342 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins.

ILI9340 supports several pixel formats that can be selected by DPI [2:0] bits of “Pixel Format Set (3Ah)” and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM[1:0]		RIM	DPI[2:0]			RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	**DE Mode** Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, DB[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[15:0]
1	0	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	**SYNC Mode** In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, DB[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB[15:0]
1	1	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, DB[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB[5:0]

18-bit data bus interface (D[17:0] is used) , DPI[2:0] = 110, and RIM=0

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[15:0] is used) , DPI[2:0] = 101, and RIM=0

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 110, and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 101, and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

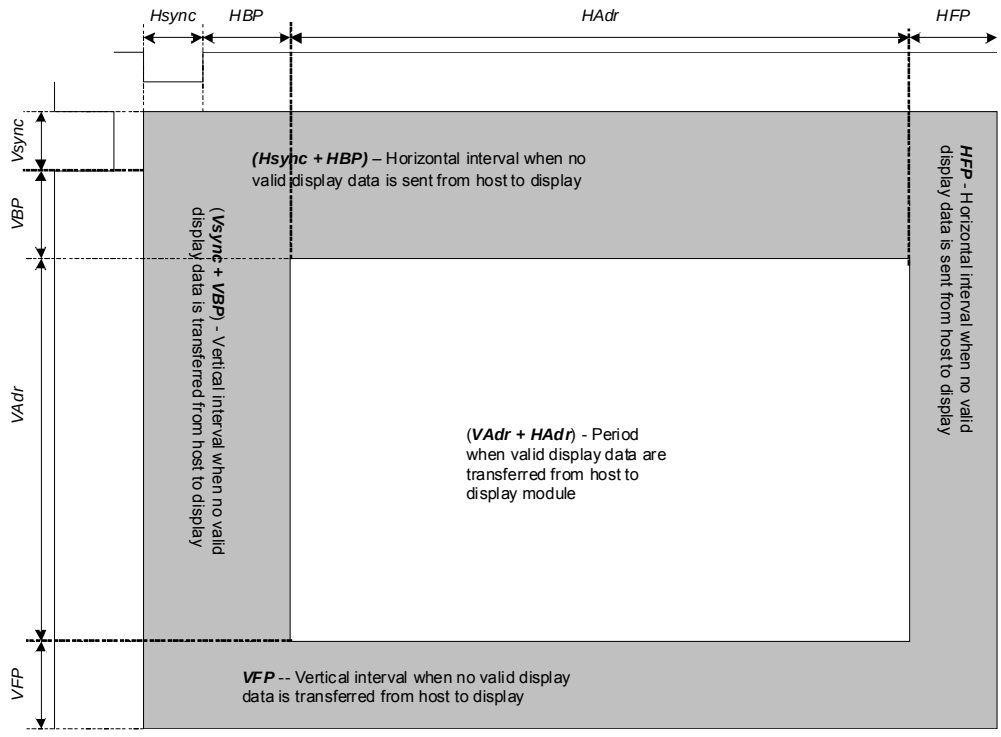
The LSB data of red/blue color depends on the EPF[1:0] setting.

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as continues internal

clock for other functions of the display module. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of DOTCLK). D [17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	320	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Typical values are setting example when used with panel resolution 320 x 240 (LQVGA), clock frequency 5.31MHz and frame frequency about 60Hz.

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

(Number of PCLK per 1 line) ≥ (Number of RTN clock) x Division ratio (DIV) x (PCDIVL+PCDIVH)

Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

PCDIVH [3:0]: Number of DOTCLK during internal clock CLKD's high period. In units of 1 clock.

PCDIVL [3:0]: Number of DOTCLK during internal clock CLKD's low period. In units of 1 clock.

PCDIVH and PCDIVL, specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 678KHz is the smallest. Set PCDIVL = PCDIVH or PCDIVL - 1. Follow the restriction (Number of PCLK in 1H) ≥ (Number of RTN clock) * (Division ratio (DIV)) * (PCDIVL + PCDIVH).

Setting Example: To set frame frequency to 60Hz:

Internal Clock

Internal Oscillation Clock: 236KHz

DIV[1:0] = 2'b0 (x 1/1)

RTN[4:0] = 5'h10 (16 clocks)

FP = 8'h4 (4 lines), BP = 8'h2 (2 lines), NL = 6'h1D (240 lines)

236KHz/1/(240+2+4)/16 = 59.95 Hz

Frame Rate → 59.95Hz

DOTCLK

HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

60Hz x (2 + 240 + 4) lines x (10 + 20 + 320 + 10) clocks = 5.31MHz

DOTCLK frequency = 5.31MHz

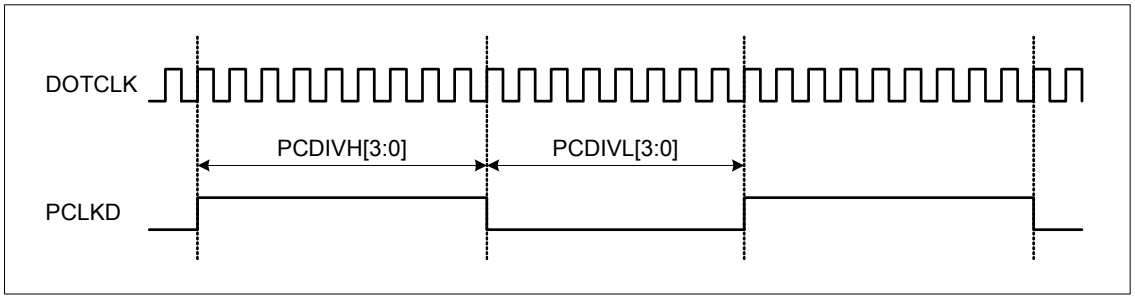
5.31 MHz / 236KHz = 22.5 □ Set PCDIVH and PCDIVL so that PCLK is divided by 22.

5.31 MHz / 22 = 241KHz

241KHz / 16 clocks / 246 lines = 61.22Hz

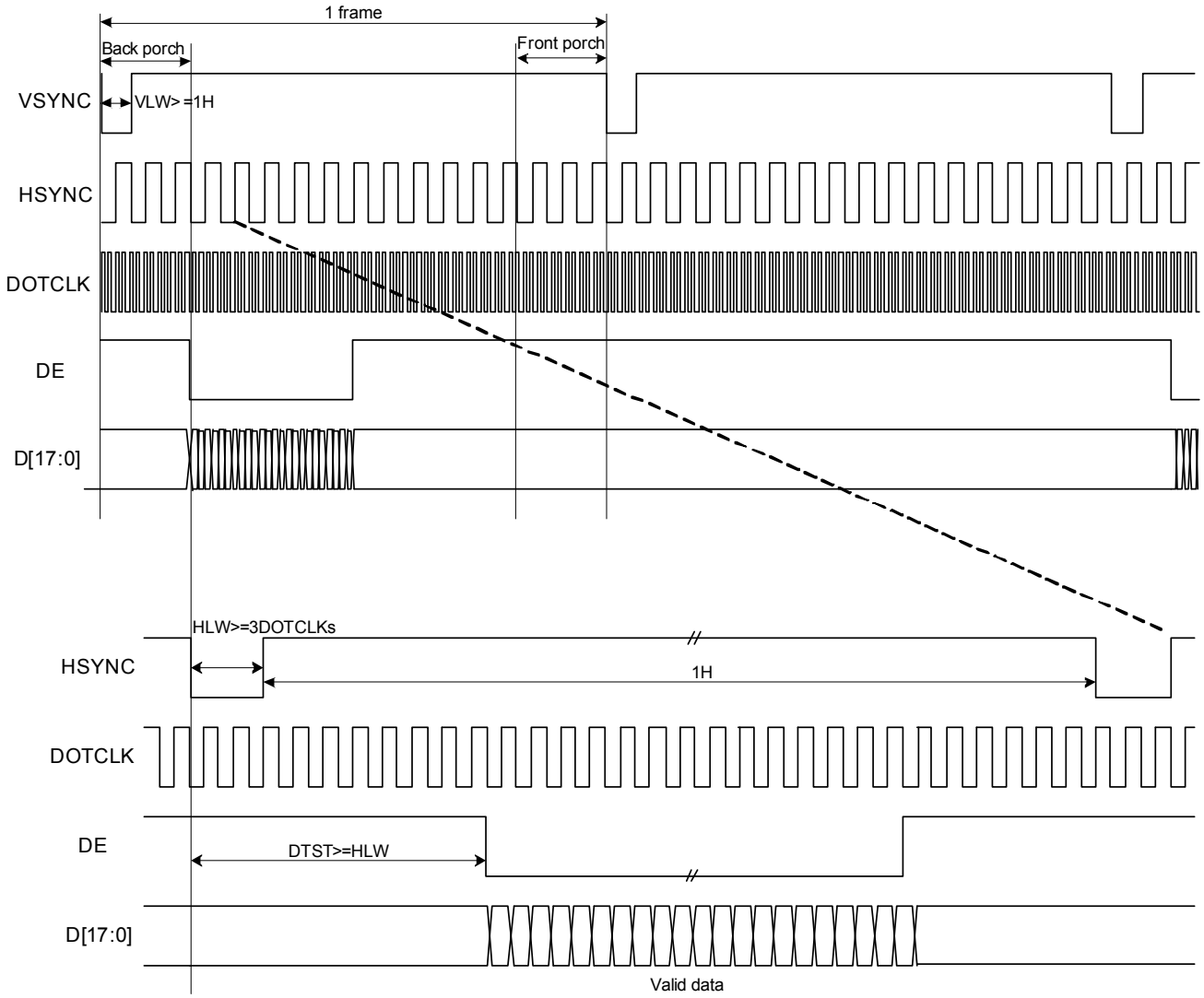
PCDIVH[3:0] = 4'hB (11 DOTCLK)

PCDIVL[3:0] = 4'hB (11 DOTCLK)



7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

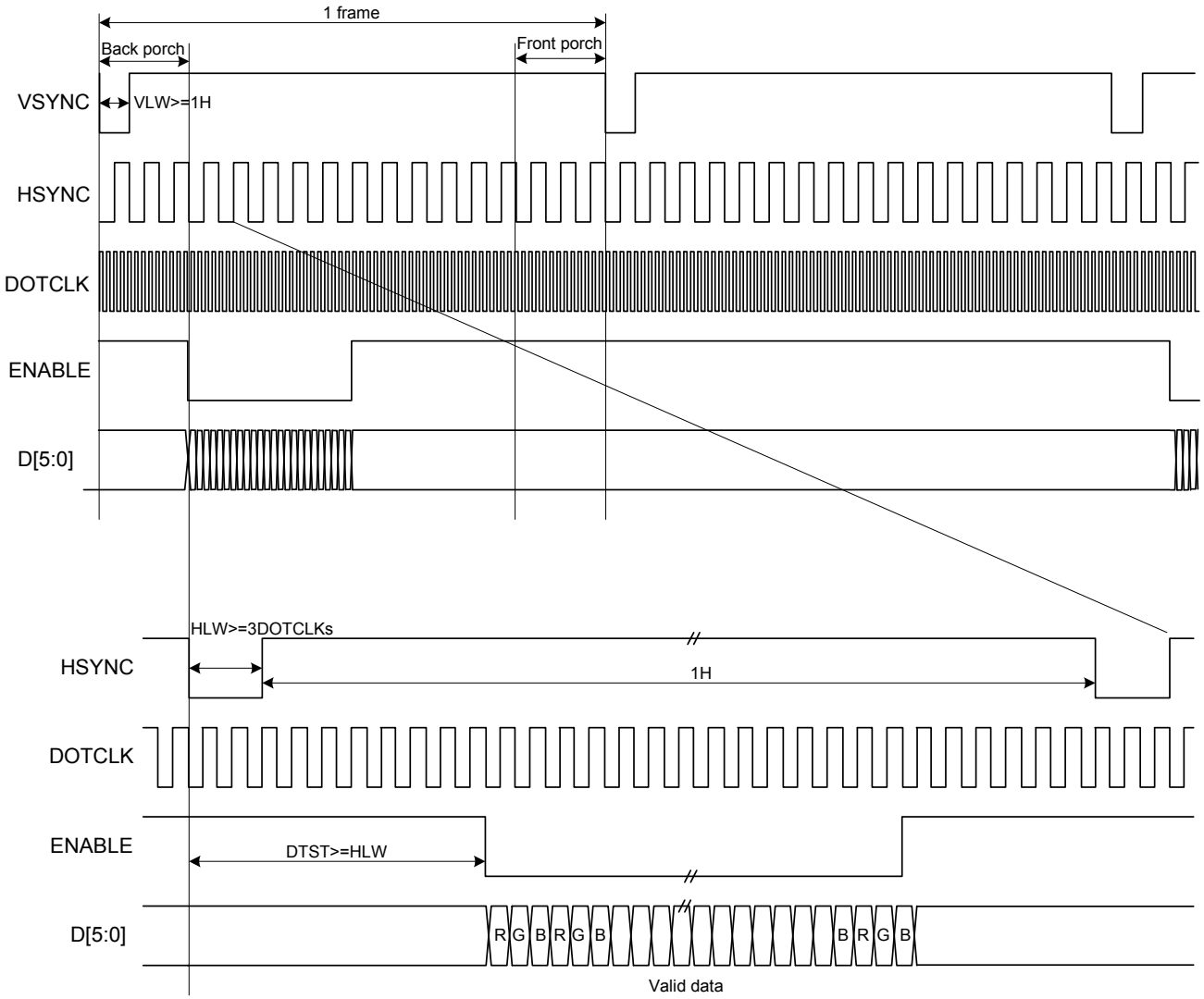


VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

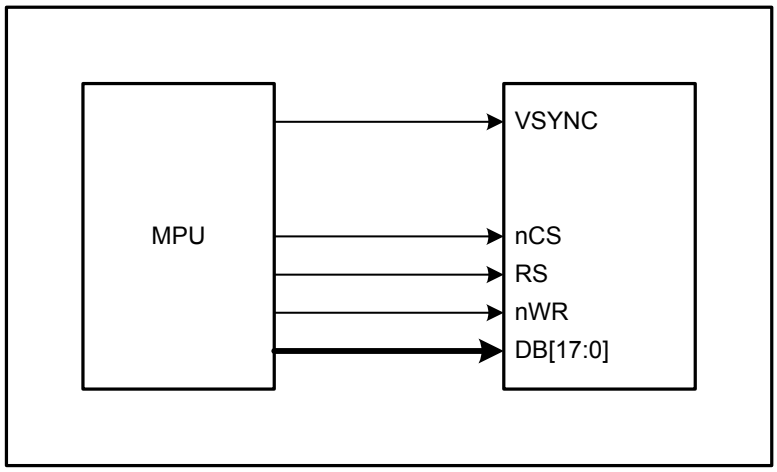
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

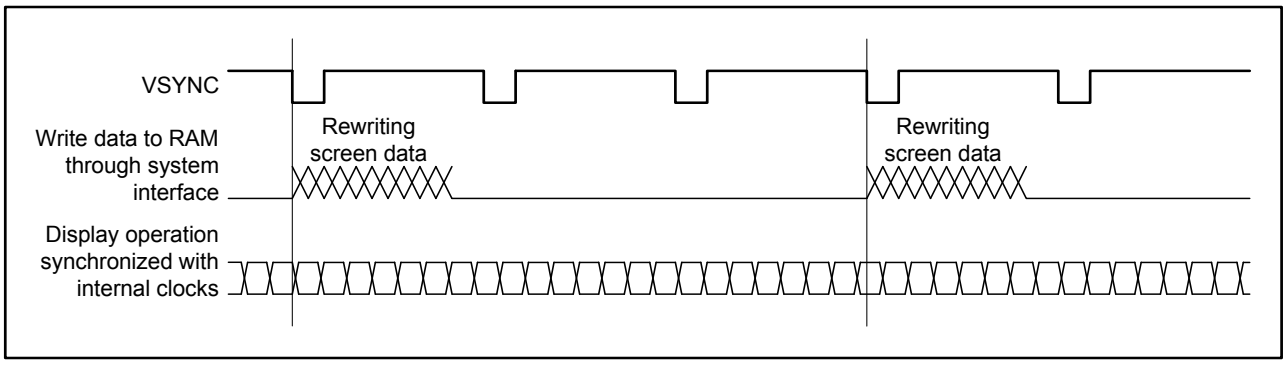
Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

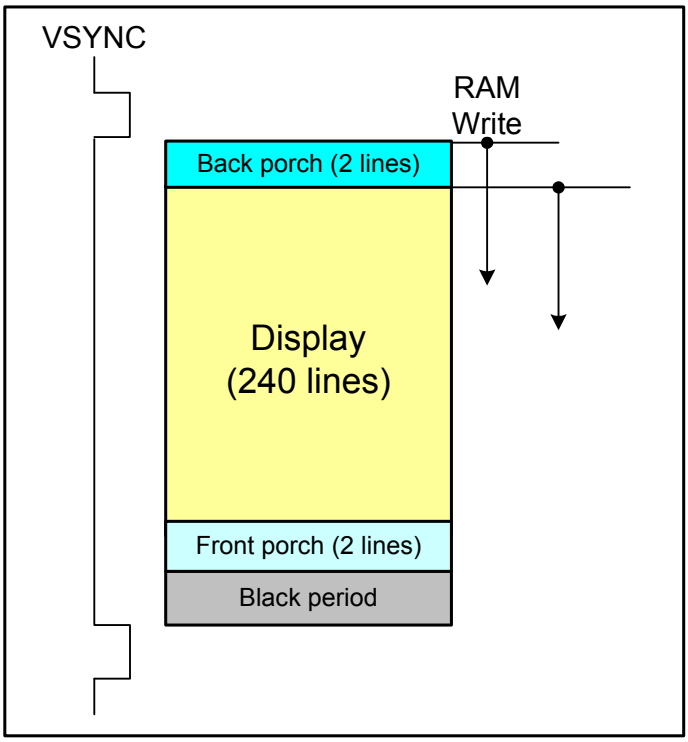
7.3. VSYNC Interface

ILI9342 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080/6800 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.



In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed [Hz]} > \frac{240 \times DisplayLines(NL)}{[BackPorch(VBP) + DisplayLines(NL) - margins] \times Clocks\ per\ line \times (1/fosc)}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 320 RGB × 240 lines

Lines: 240 lines (NL = 011101)

Back porch: 2 lines (VBP = 0000010)

Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz

Frequency fluctuation: 10%

Clocks per line : 16 clocks

Internal oscillator clock (fosc.) [Hz] = 70 x [240+ 2 + 2] x 16 clocks x (1.1/0.9) ≒ 334KHz

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

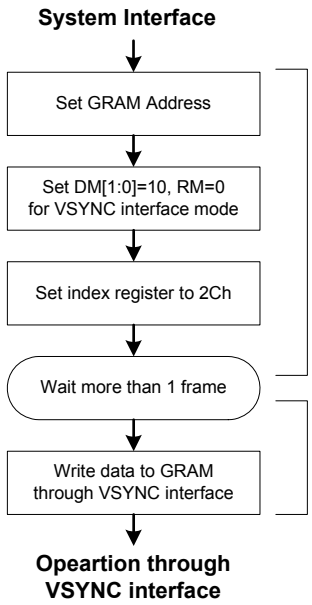
Minimum speed for RAM writing [Hz] > 320 x 240 x 334K / [(2 + 240 + 2)lines x 16clocks] ≒ 6.57 MHz

The above theoretical value is calculated based on the premise that the ILI9342 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.57MHz or more will guarantee the completion of GRAM write operation before the ILI9342 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

System Interface Mode to VSYNC interface mode

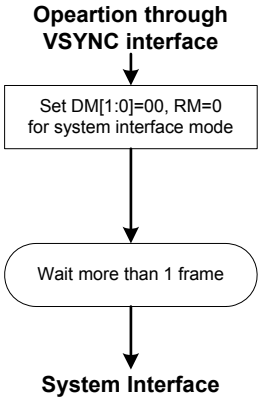


Display operation in synchronization with internal clocks

DM[1:0], RM become enable after completion of displaying 1 frame

Display operation in synchronization with VSYNC

VSYNC interface mode to System Interface Mode



Display operation in synchronization with VSYNC

DM[1:0], RM become enable after completion of displaying 1 frame

Display operation in synchronization with internal clocks

Note: input VSYNC for more than 1 frame period after setting the DM, RM register.

7.4. Color Depth Conversion Look-Up Table

When ILI9342 operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel –mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	1
00001	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	2
00010	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	3
00011	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	4
00100	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	5
00101	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	6
00110	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	7
00111	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	8
01000	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	9
01001	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	10
01010	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	11
01011	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	12
01100	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	13
01101	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	14
01110	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	15
01111	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	16
10000	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	17
10001	R_{175} R_{174} R_{173} R_{172} R_{171} R_{170}	18
10010	R_{185} R_{184} R_{183} R_{182} R_{181} R_{180}	19
10011	R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}	20
10100	R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}	21
10101	R_{215} R_{214} R_{213} R_{212} R_{211} R_{210}	22
10110	R_{225} R_{224} R_{223} R_{222} R_{221} R_{220}	23
10111	R_{235} R_{234} R_{233} R_{232} R_{231} R_{230}	24
11000	R_{245} R_{244} R_{243} R_{242} R_{241} R_{240}	25
11001	R_{255} R_{254} R_{253} R_{252} R_{251} R_{250}	26
11010	R_{265} R_{264} R_{263} R_{262} R_{261} R_{260}	27
11011	R_{275} R_{274} R_{273} R_{272} R_{271} R_{270}	28
11100	R_{285} R_{284} R_{283} R_{282} R_{281} R_{280}	29
11101	R_{295} R_{294} R_{293} R_{292} R_{291} R_{290}	30
11110	R_{305} R_{304} R_{303} R_{302} R_{301} R_{300}	31
11111	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	32

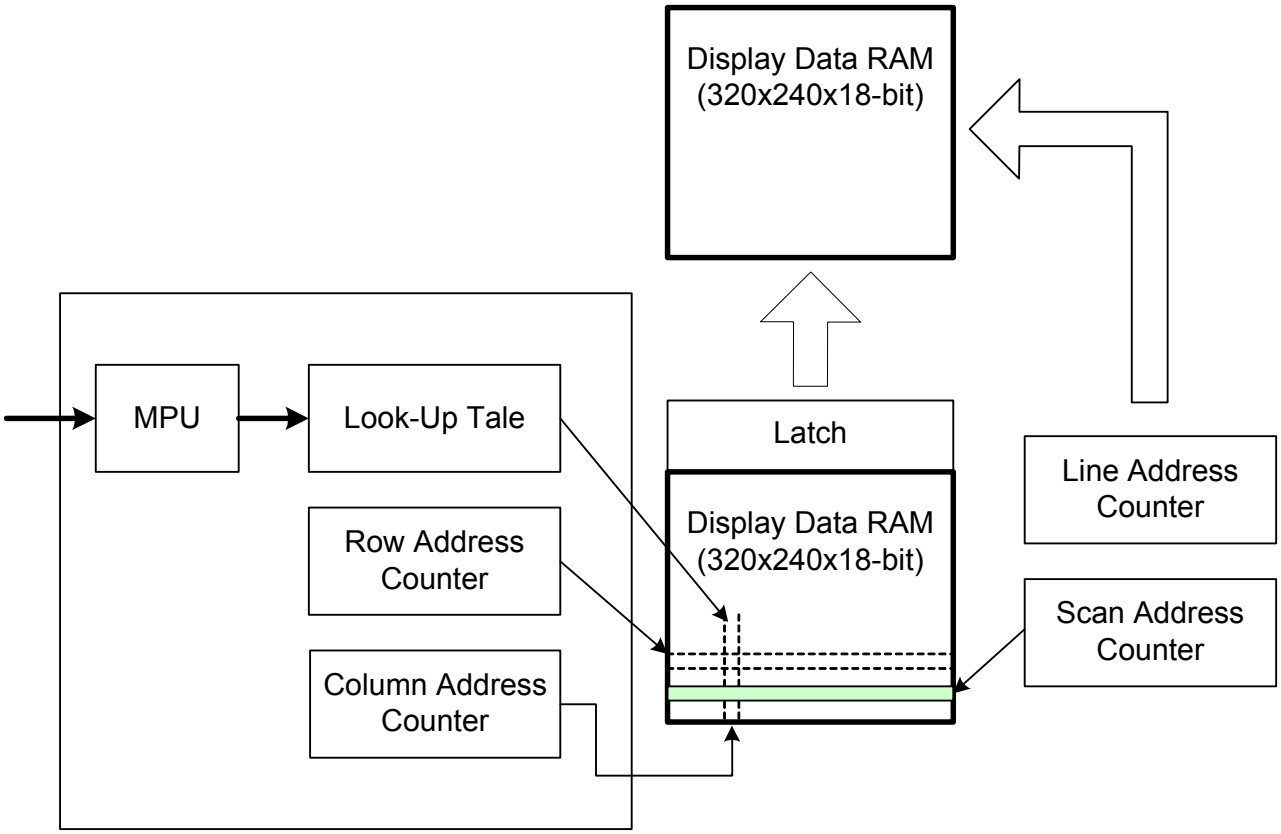
G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	33
000001	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	34
000010	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	35
000011	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	36
000100	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	37
000101	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	38
000110	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	39
000111	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	40
001000	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	41
001001	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	42
001010	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	43
001011	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	44
001100	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	45
001101	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	46
001110	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	47
001111	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	48
010000	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	49
010001	G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}	50
010010	G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}	51
010011	G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}	52
010100	G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}	53
010101	G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}	54
010110	G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}	55
010111	G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}	56
011000	G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}	57
011001	G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}	58
011010	G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}	59
011011	G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}	60
011100	G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}	61
011101	G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}	62
011110	G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}	63
011111	G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}	64
100000	G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}	65
100001	G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}	66

G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}	67
100011	G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}	68
100100	G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}	69
100101	G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}	70
100110	G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}	71
100111	G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}	72
101000	G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}	73
101001	G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}	74
101010	G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}	75
101011	G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}	76
101100	G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}	77
101101	G_{455} G_{454} G_{453} G_{452} G_{451} G_{450}	78
101110	G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}	79
101111	G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}	80
110000	G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}	81
110001	G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}	82
110010	G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}	83
110011	G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}	84
110100	G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}	85
110101	G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}	86
110110	G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}	87
110111	G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}	88
111000	G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}	89
111001	G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}	90
111010	G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}	91
111011	G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}	92
111100	G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}	93
111101	G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}	94
111110	G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}	95
111111	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}	96

B input (5-bit) 16-bit/pixel –mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B_{005} B_{004} B_{003} B_{002} B_{001} B_{000}	97
00001	B_{015} B_{014} B_{013} B_{012} B_{011} B_{010}	98
00010	B_{025} B_{024} B_{023} B_{022} B_{021} B_{020}	99
00011	B_{035} B_{034} B_{033} B_{032} B_{031} B_{030}	100
00100	B_{045} B_{044} B_{043} B_{042} B_{041} B_{040}	101
00101	B_{055} B_{054} B_{053} B_{052} B_{051} B_{050}	102
00110	B_{065} B_{064} B_{063} B_{062} B_{061} B_{060}	103
00111	B_{075} B_{074} B_{073} B_{072} B_{071} B_{070}	104
01000	B_{085} B_{084} B_{083} B_{082} B_{081} B_{080}	105
01001	B_{095} B_{094} B_{093} B_{092} B_{091} B_{090}	106
01010	B_{105} B_{104} B_{103} B_{102} B_{101} B_{100}	107
01011	B_{115} B_{114} B_{113} B_{112} B_{111} B_{110}	108
01100	B_{125} B_{124} B_{123} B_{122} B_{121} B_{120}	109
01101	B_{135} B_{134} B_{133} B_{132} B_{131} B_{130}	110
01110	B_{145} B_{144} B_{143} B_{142} B_{141} B_{140}	111
01111	B_{155} B_{154} B_{153} B_{152} B_{151} B_{150}	112
10000	B_{165} B_{164} B_{163} B_{162} B_{161} B_{160}	113
10001	B_{175} B_{174} B_{173} B_{172} B_{171} B_{170}	114
10010	B_{185} B_{184} B_{183} B_{182} B_{181} B_{180}	115
10011	B_{195} B_{194} B_{193} B_{192} B_{191} B_{190}	116
10100	B_{205} B_{204} B_{203} B_{202} B_{201} B_{200}	117
10101	B_{215} B_{214} B_{213} B_{212} B_{211} B_{210}	118
10110	B_{225} B_{224} B_{223} B_{222} B_{221} B_{220}	119
10111	B_{235} B_{234} B_{233} B_{232} B_{231} B_{230}	120
11000	B_{245} B_{244} B_{243} B_{242} B_{241} B_{240}	121
11001	B_{255} B_{254} B_{253} B_{252} B_{251} B_{250}	122
11010	B_{265} B_{264} B_{263} B_{262} B_{261} B_{260}	123
11011	B_{275} B_{274} B_{273} B_{272} B_{271} B_{270}	124
11100	B_{285} B_{284} B_{283} B_{282} B_{281} B_{280}	125
11101	B_{295} B_{294} B_{293} B_{292} B_{291} B_{290}	126
11110	B_{305} B_{304} B_{303} B_{302} B_{301} B_{300}	127
11111	B_{315} B_{314} B_{313} B_{312} B_{311} B_{310}	128

7.5. Display Data RAM (DDRAM)

ILI9342 has an integrated 320x240x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 320xRGBx240 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

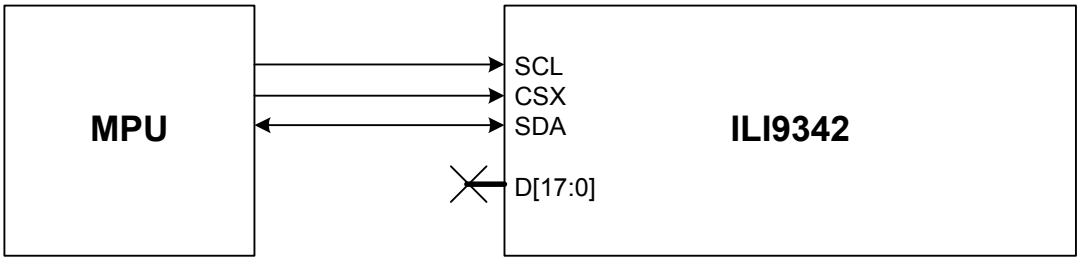


7.6. Display Data Format

ILI9342 supplies 18-/16-/9-/8-bit parallel MPU interface with 8080/6800-series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MPU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.6.1. 3-line Serial Interface

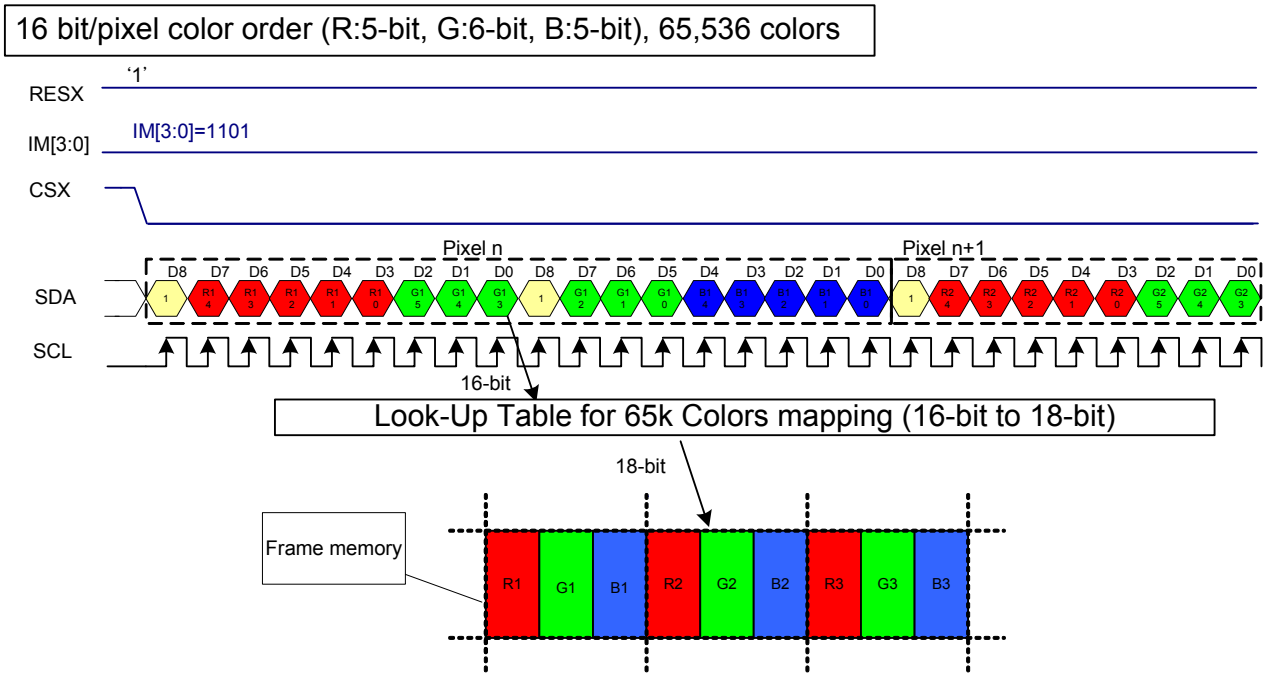
The 3-line/9-bit serial bus interface of ILI9342 can be used by setting external pin as IM [3:0] to “1101”. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.



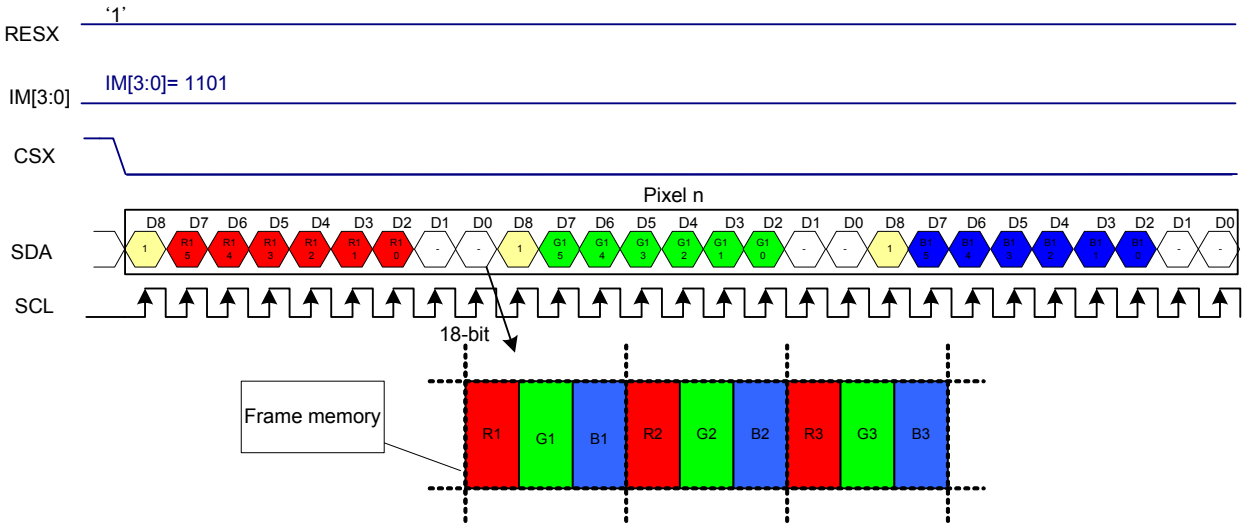
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



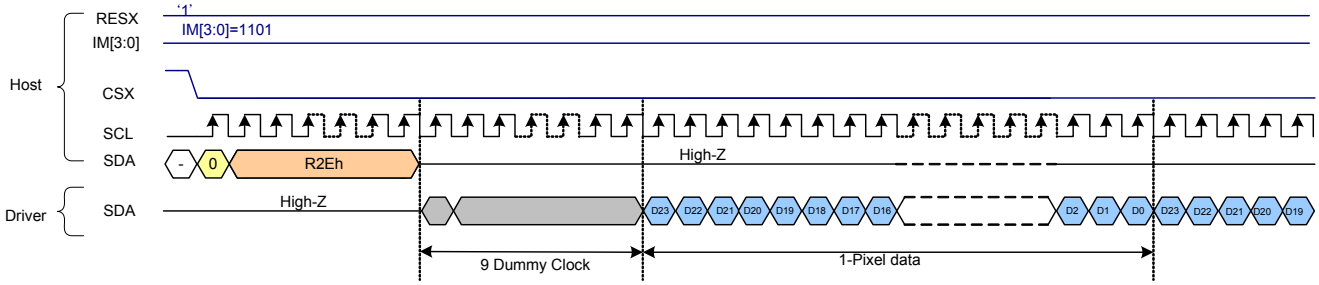
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

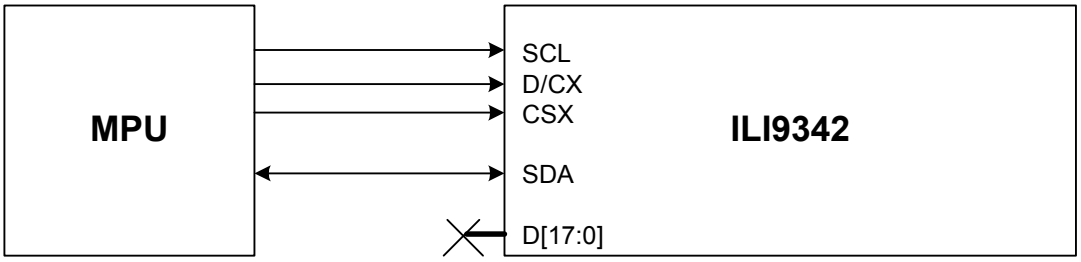
Read data through 3-line SPI mode



Note 1: '-'= Don't care –Can be set "0" or "1".

7.6.2. 4-line Serial Interface

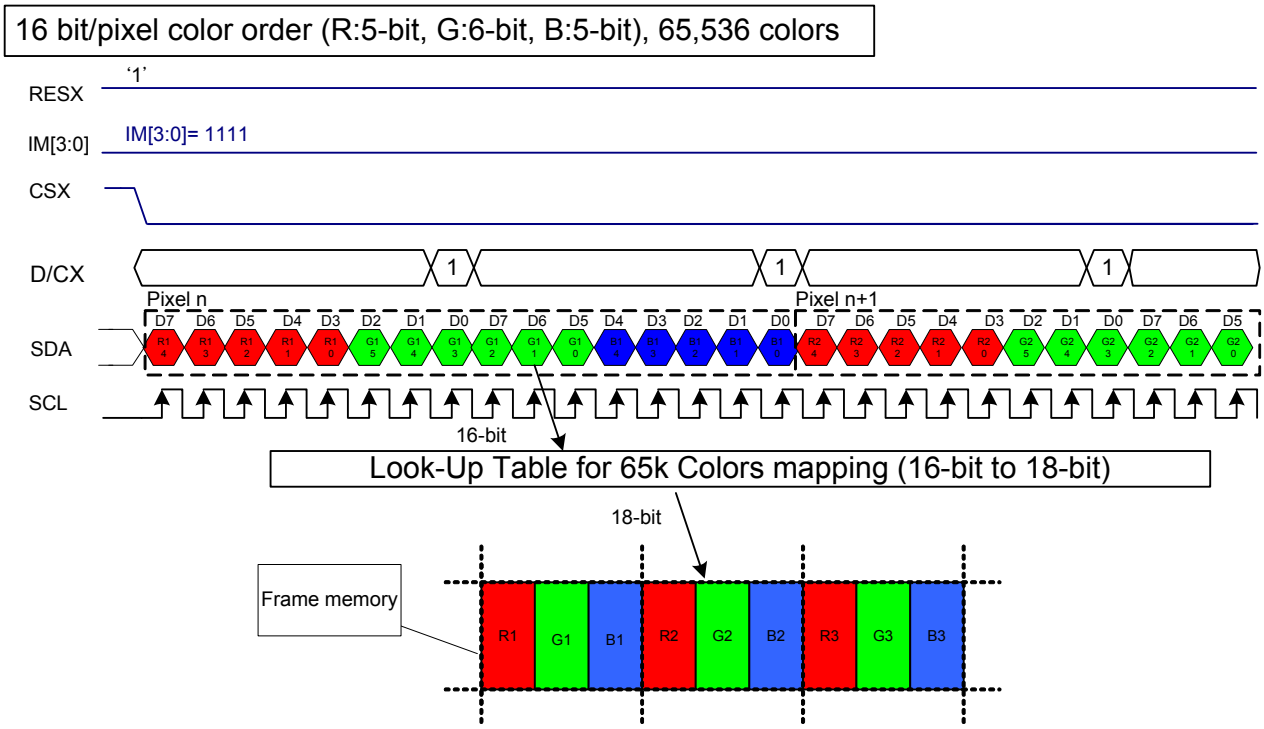
The 4-line/8-bit serial bus interface of ILI9342 can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.



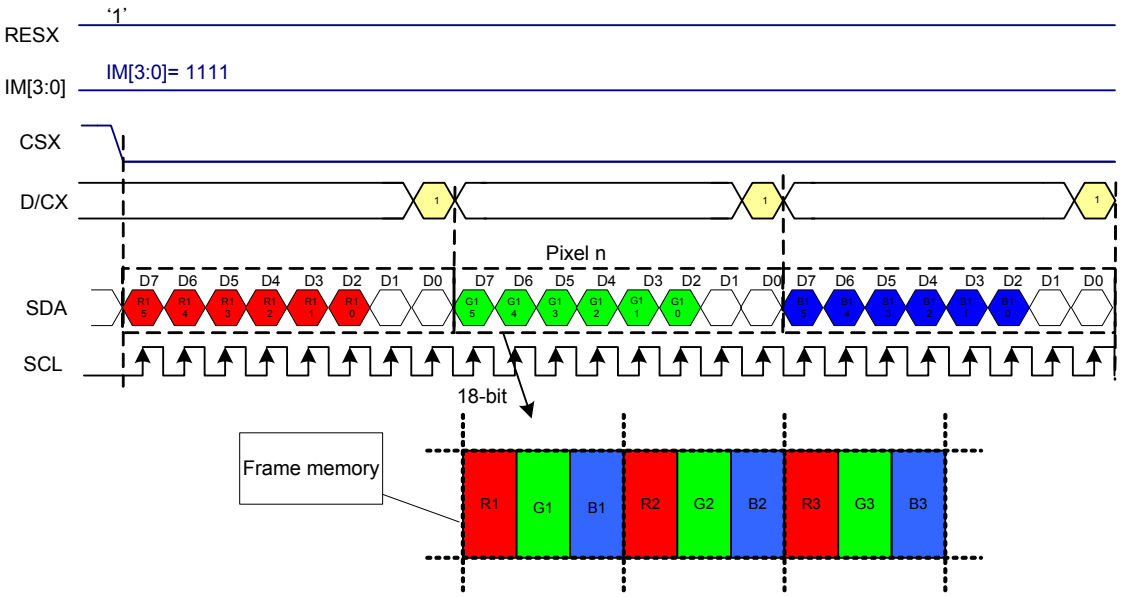
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



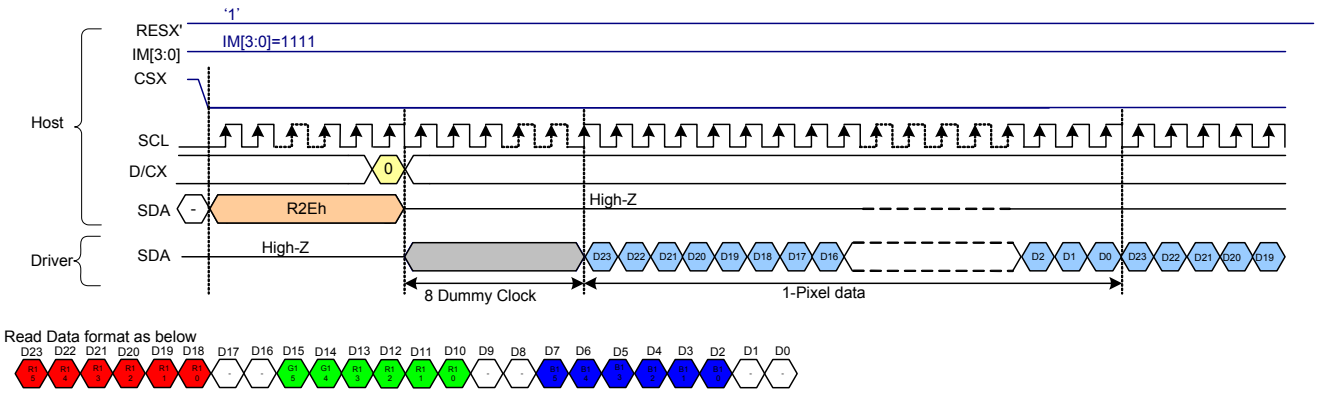
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Read data through 4-line SPI mode

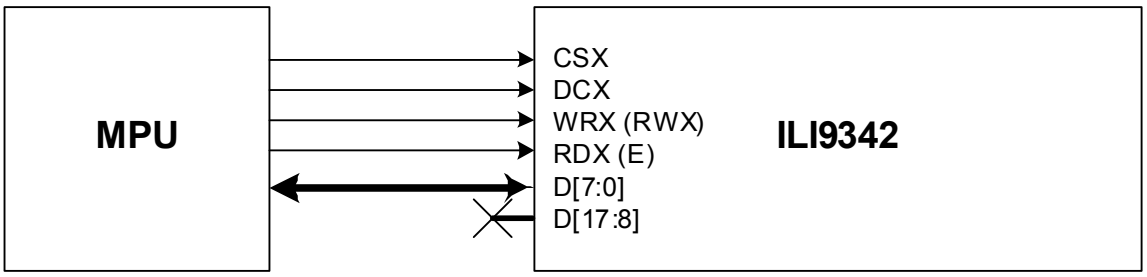


Read Data format as below

Note 1: '-'= Don't care – Can be set "0" or "1".

7.6.3. 8-bit Parallel MPU Interface

The 8080-system 8-bit parallel bus interface of ILI9640 can be used by setting external pin as IM [3:0] to “0100”. And the 6800-system 8-bit parallel bus interface mode can be used by settings as IM [3:0] =”0000”. The figure in the following is the example of interface with 8080/6800 microcomputer system interface.

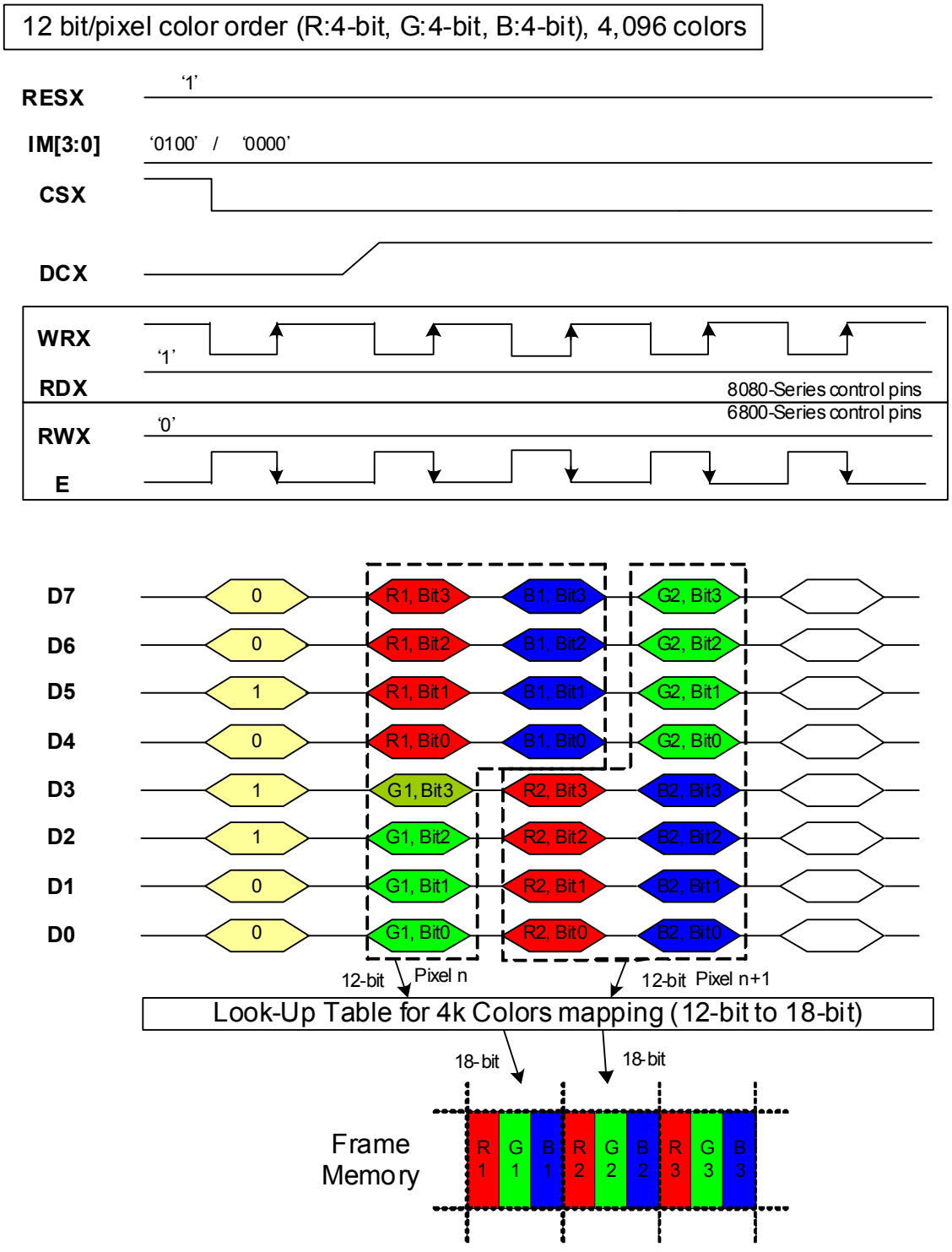


Different display data formats are available for four color depths supported by listed below.

- 4K-Colors, RGB 4, 4, 4 -bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.6.3.1. 8-bit Data Bus for 12-bit/pixel (RGB 4-4-4 bits input), 4K-color

There is 2 pixels display data per 3-bytes transfer when DBI [2:0] bits are set to “011”.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

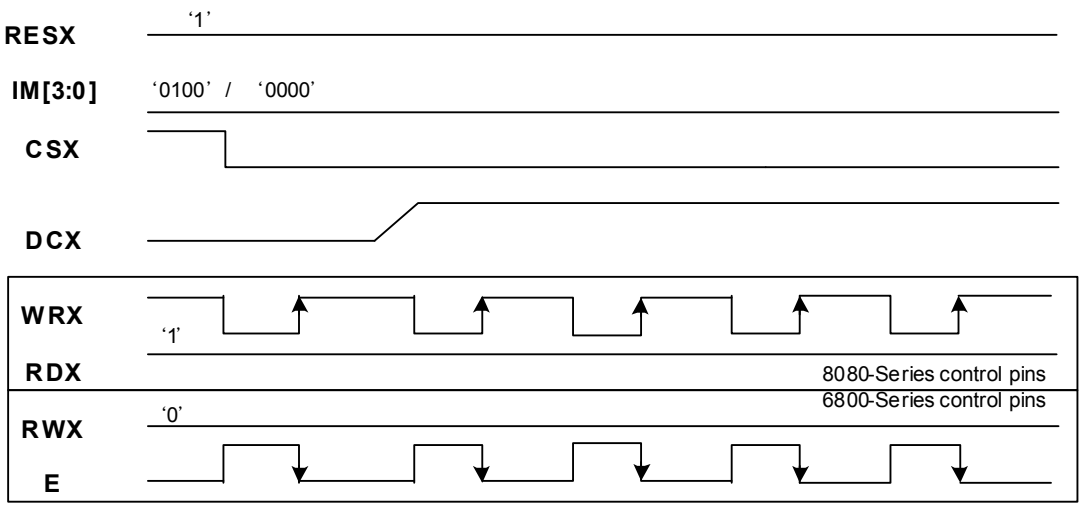
Note 2: 3-times transfer is used to transmit 2 pixel data with the 12-bits color depth information.

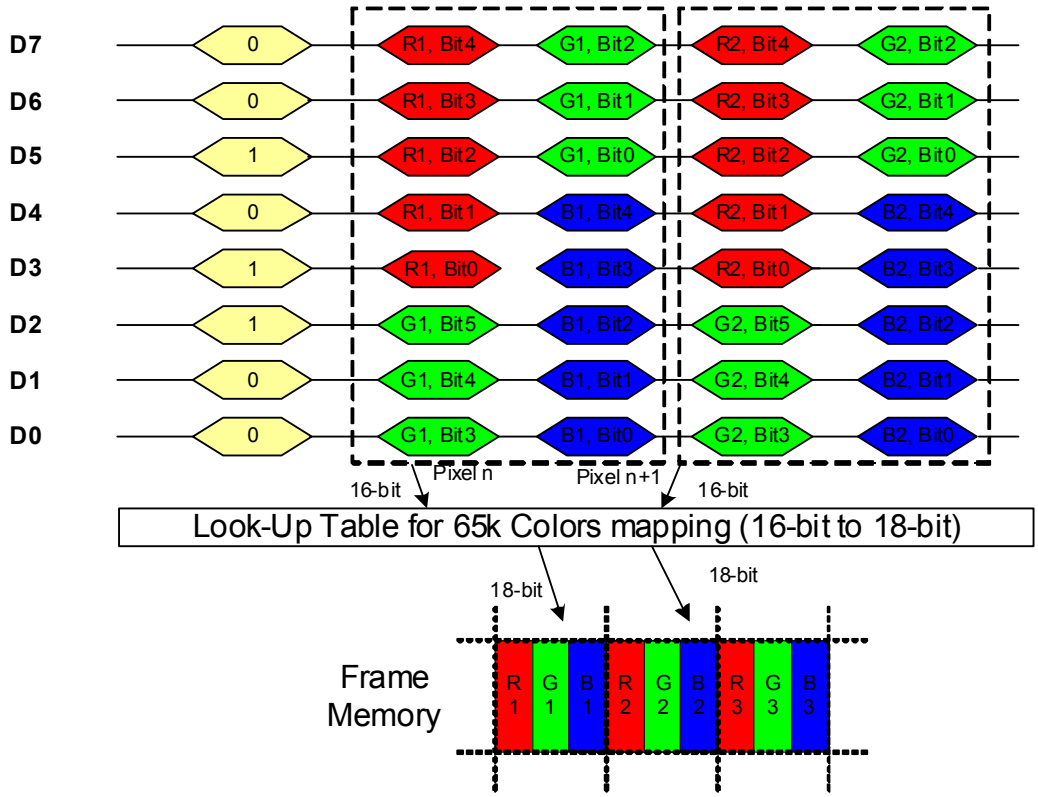
Note 3: '-'= Don't care – Leave these pins to Open.

7.6.3.2. 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

There is 1 pixel (3 sub-pixels) display data per 2-bytes transfer when DBI [2:0] bits are set to "101".

16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors





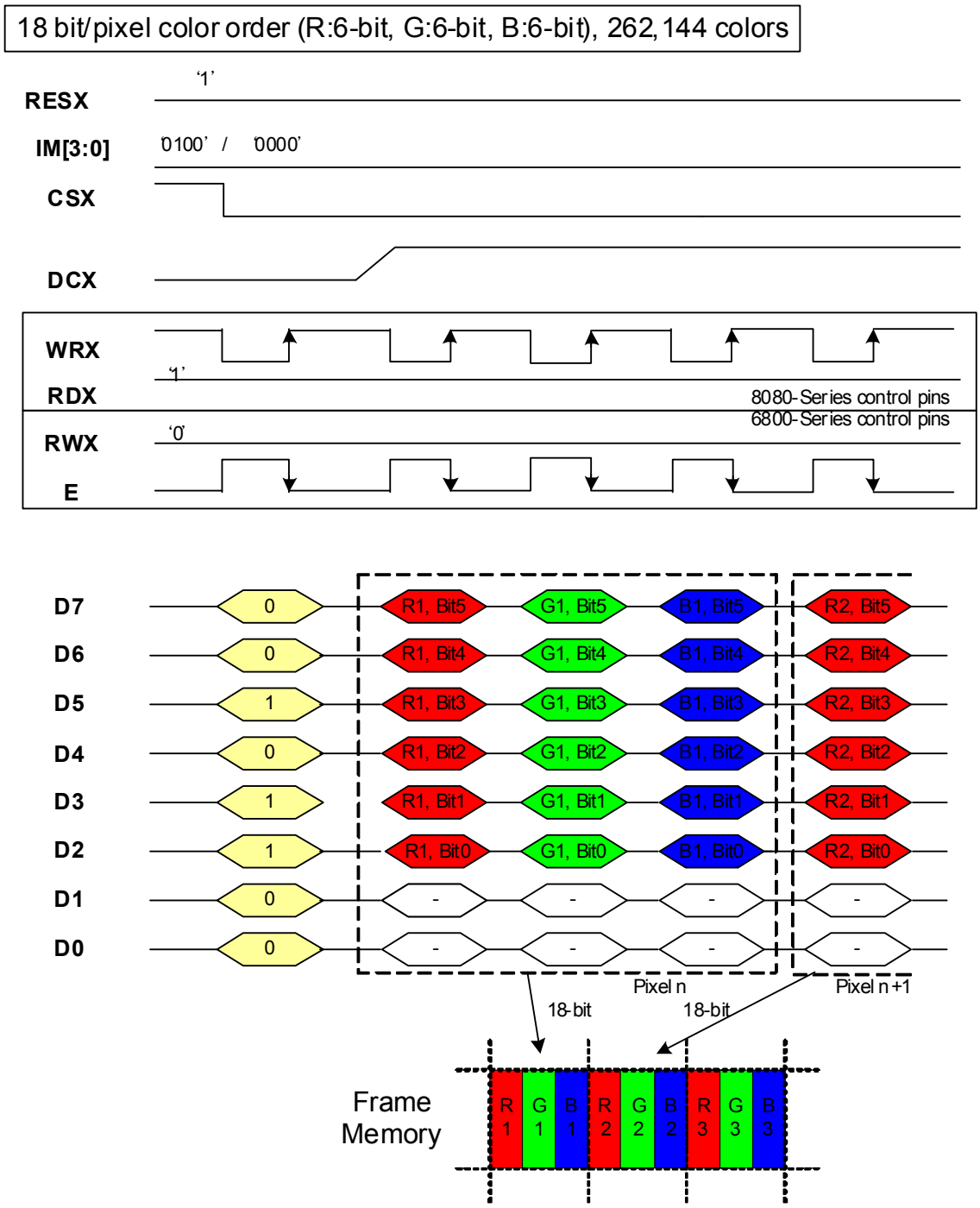
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.6.3.3. 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

There is 1 pixel (3 sub-pixels) display data per 3-bytes transfer when DBI [2:0] bits are set to "110".



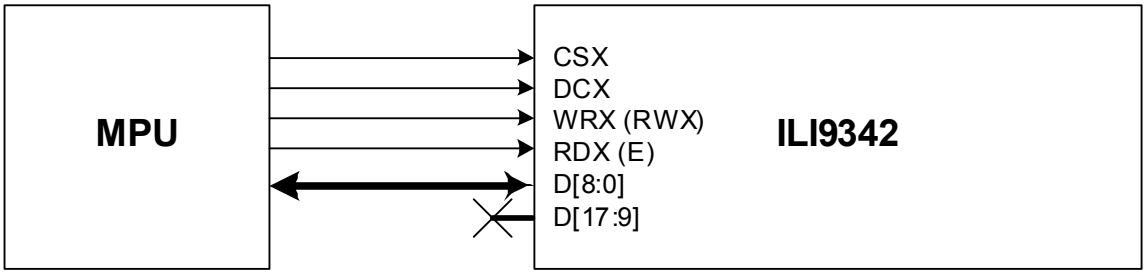
Note 1: The data order is as follows, MSB=D7, LSB=D2 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.6.4. 9-bit Parallel MPU Interface

The 8080-system 9-bit parallel bus interface of ILI9640 can be used by setting external pin as IM [3:0] to “0101”. And the 6800-system 8-bit parallel bus interface mode can be used by settings as IM [3:0] =”0001”. The figure in the following is the example of interface with 8080/6800 microcomputer system interface.



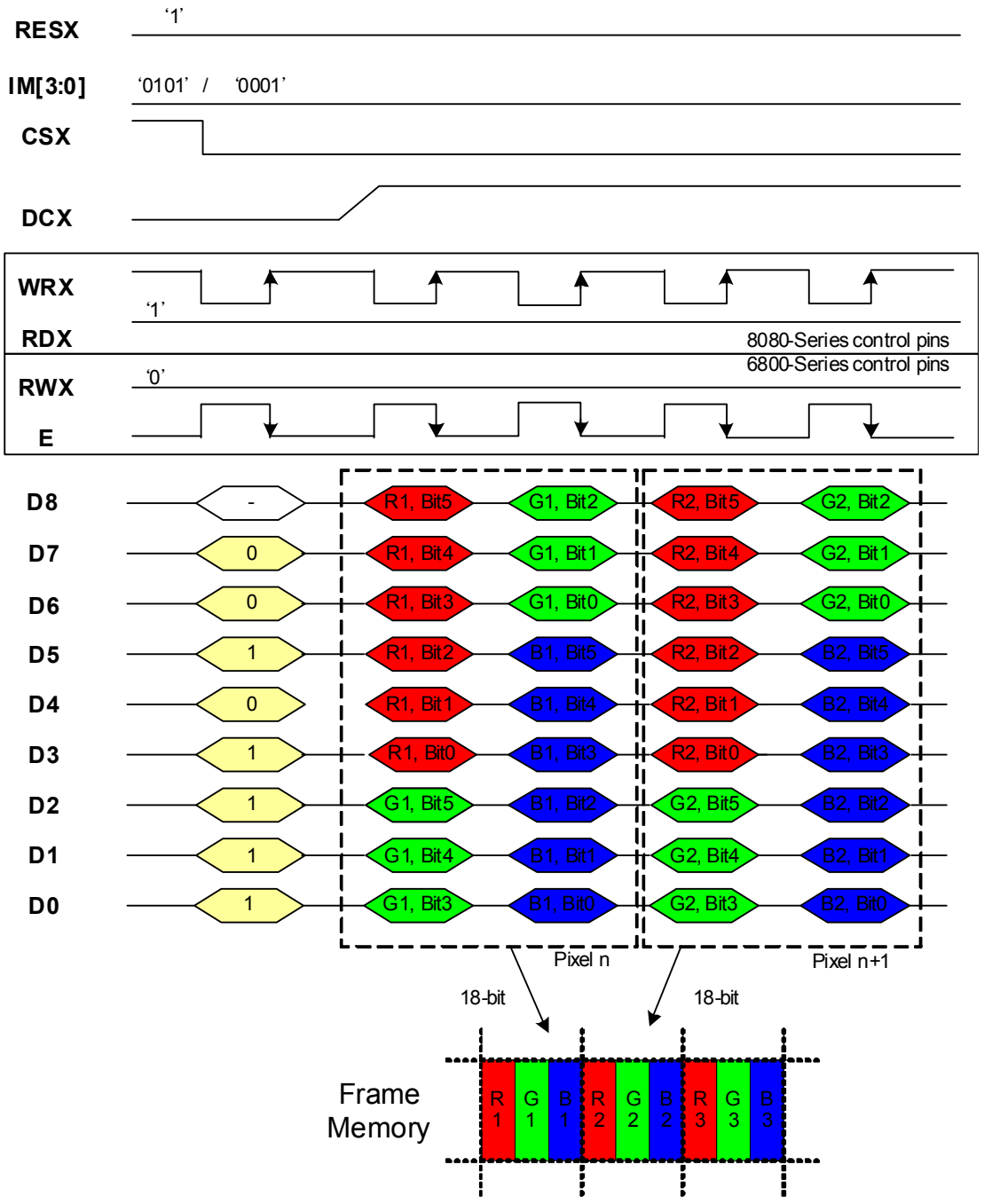
Display data format is available only for one color depth supported by listed below.

- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.6.4.1. 9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

There are 1 pixel (3 sub-pixels) display data per 2 transfers, when DBI [2:0] bits are set to “110”.

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



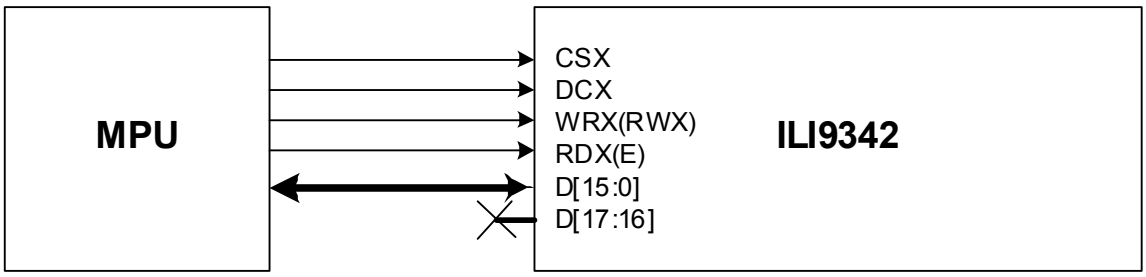
Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.6.5. 16-bit Parallel MPU Interface

The 8080-system 16-bit parallel bus interface of ILI9640 can be used by setting external pin as IM [3:0] to “0110”. And the 6800-system 16-bit parallel bus interface mode can be used by settings as IM [3:0] =”0010”. The figure in the following is the example of interface with 8080/6800 microcomputer system interface.

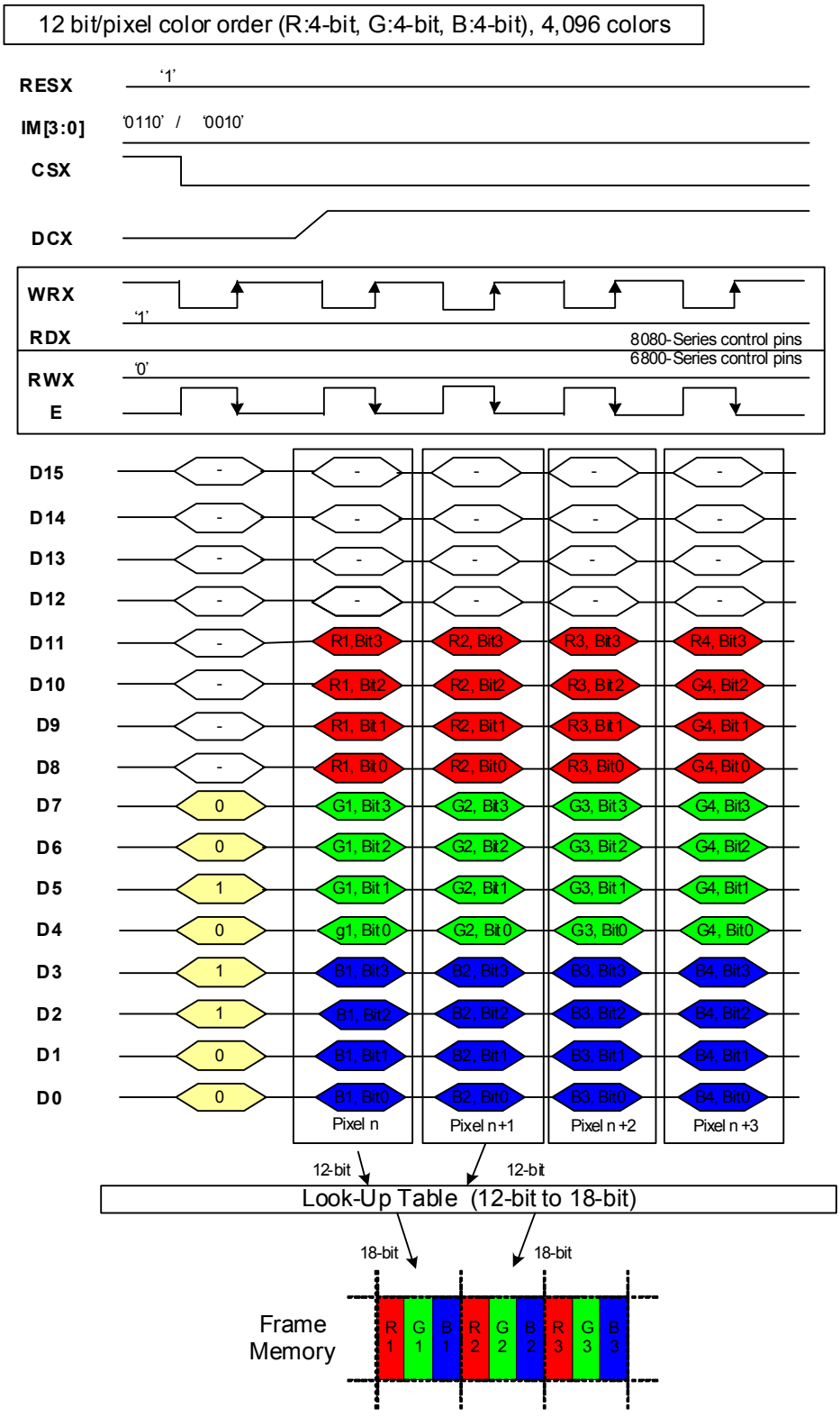


Different display data formats are available for four colors depth supported by listed below.

- 4K-Colors, RGB 4, 4, 4 -bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.6.5.1. 16-bit Data Bus for 12-bit/pixel (RGB 4-4-4 bits input), 4K-color

There is 1 pixel (3 sub-pixels) display data per 2-bytes transfer when DBI [2:0] bits are set to “011”.



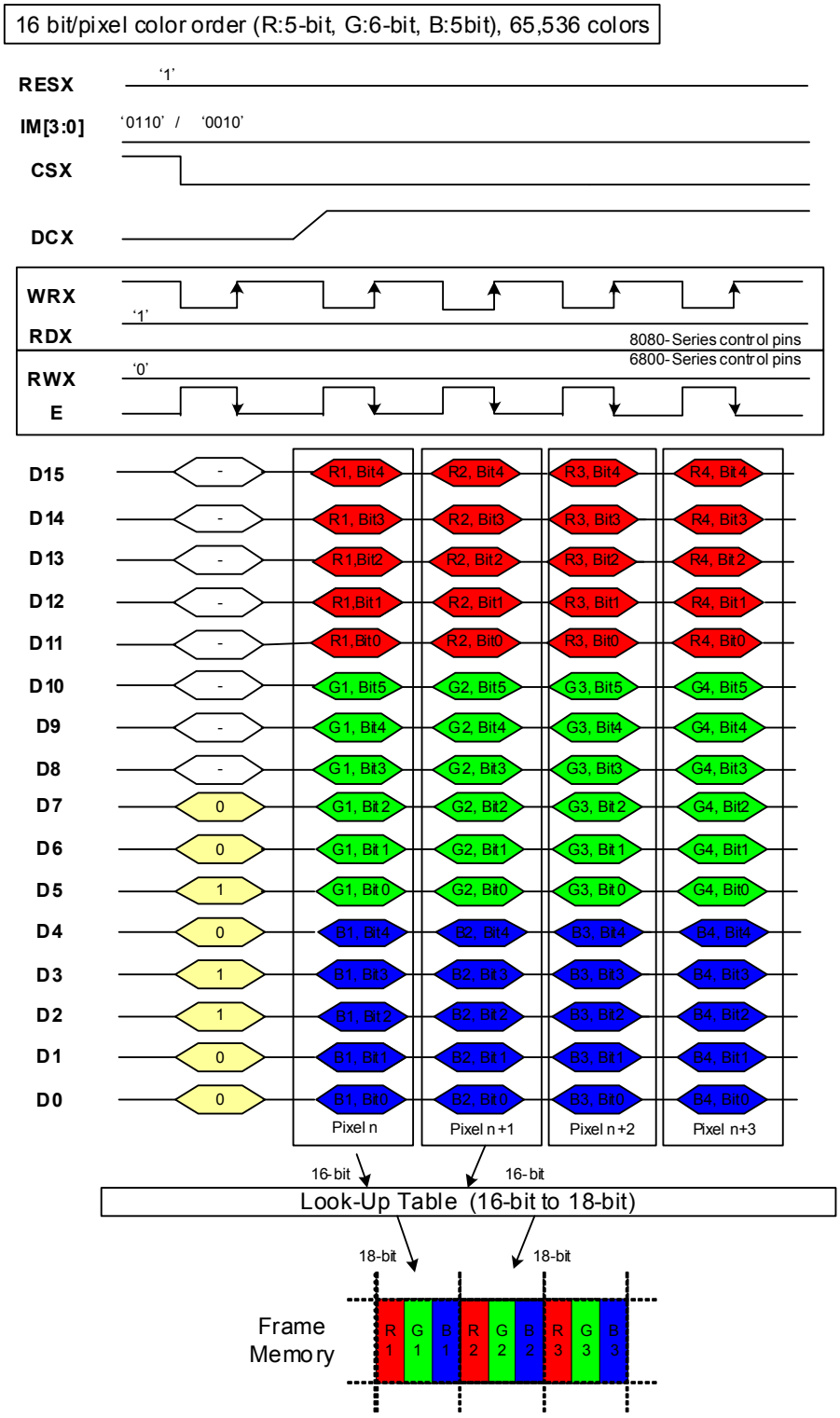
Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: ‘-‘= Don’t care – Leave these pins to Open.

7.6.5.2. 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

There is 1 pixel (3 sub-pixels) display data per 2-bytes transfer when DBI [2:0] bits are set to “101”.



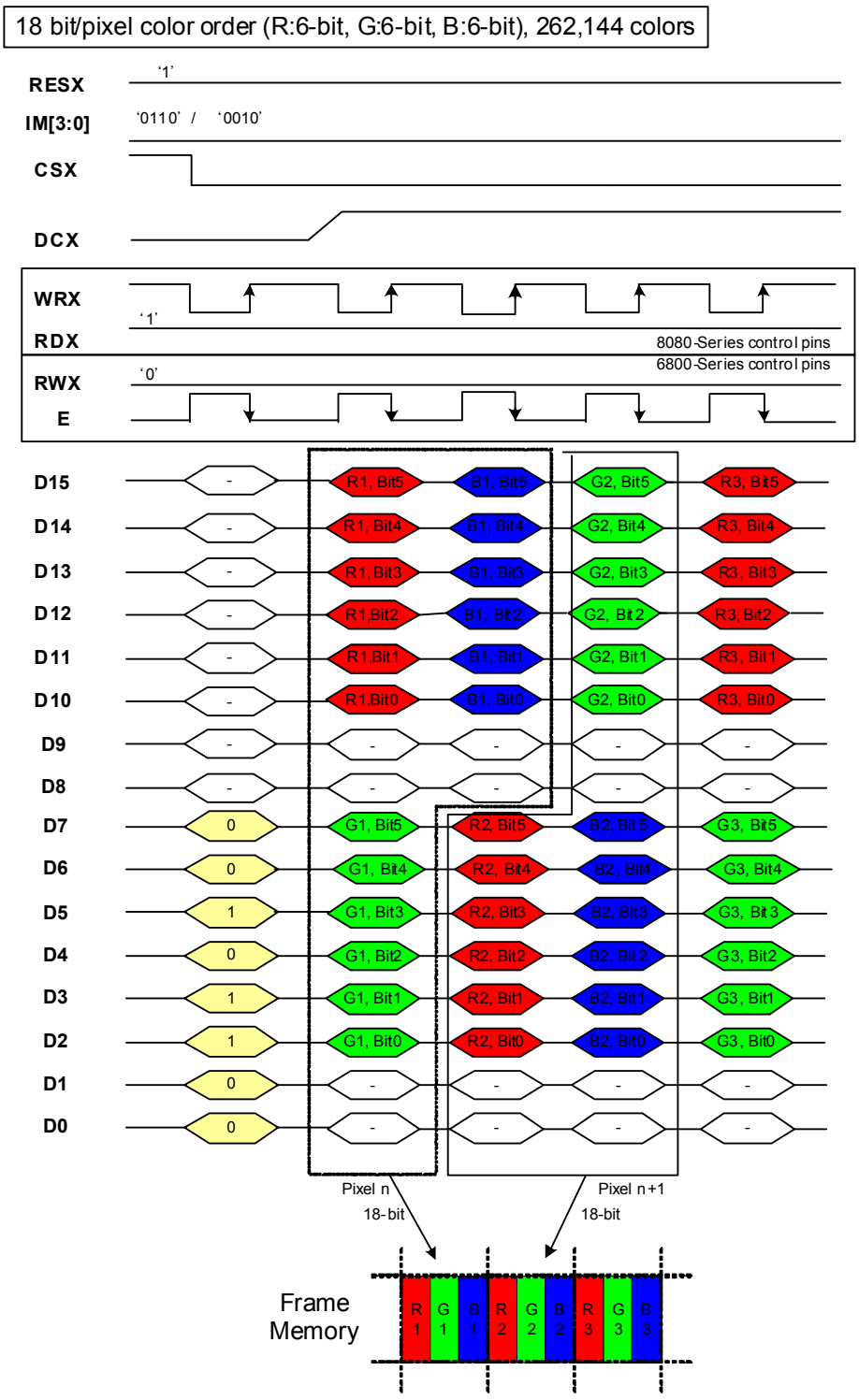
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.6.5.3. 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

There is 1 pixel (3 sub-pixels) display data per 3-bytes transfer when DBI [2:0] bits are set to “110”.



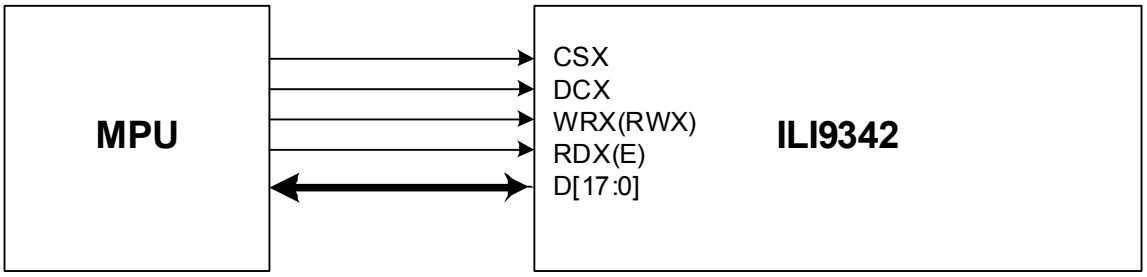
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.6.6. 18-bit Parallel MPU Interface

The 8080-system 18-bit parallel bus interface of ILI9640 can be used by setting external pin as IM [3:0] to “0111”. And the 6800-system 18-bit parallel bus interface mode can be used by settings as IM [3:0] =”0011”. The figure in the following is the example of interface with 8080/6800 microcomputer system interface.

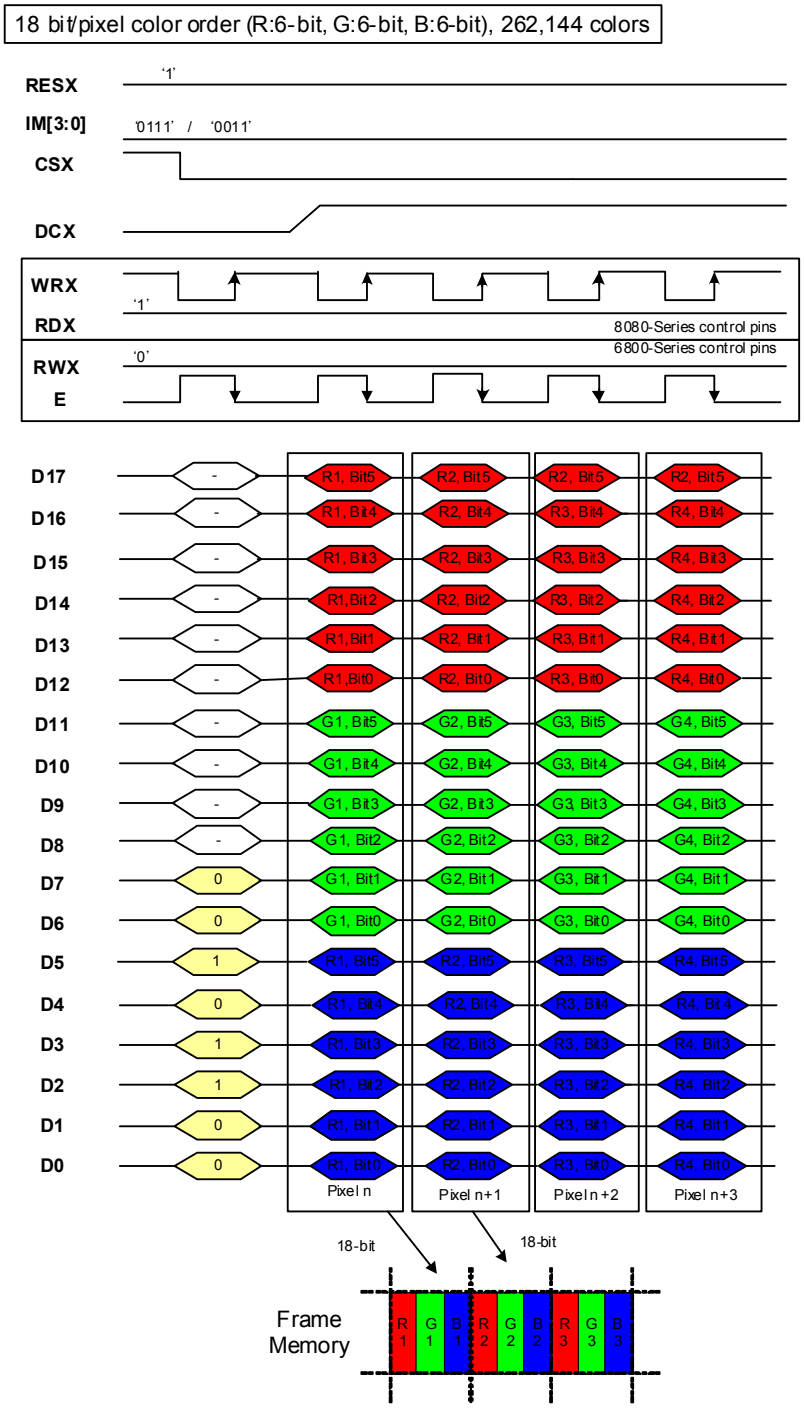


Different display data formats are available for two color depth supported by listed below.

- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.6.6.1. 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

There is 1 pixel (3 sub-pixels) display data per 1 transfer, when DBI [2:0] bits are set to “110”



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

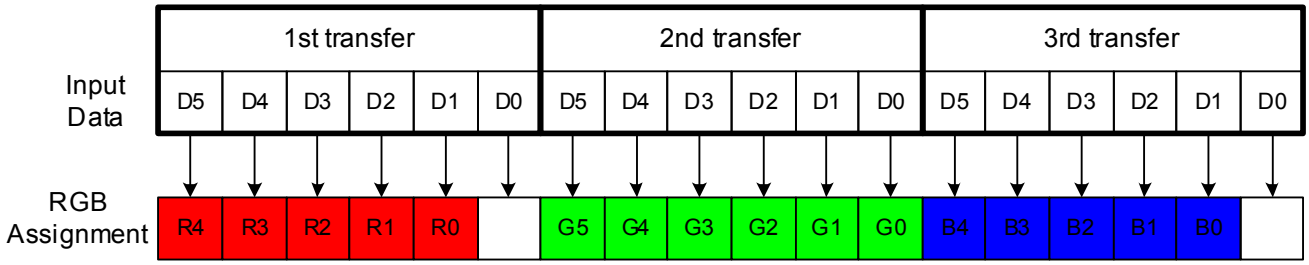
Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: ‘-‘= Don’t care – Leave these pins to Open.

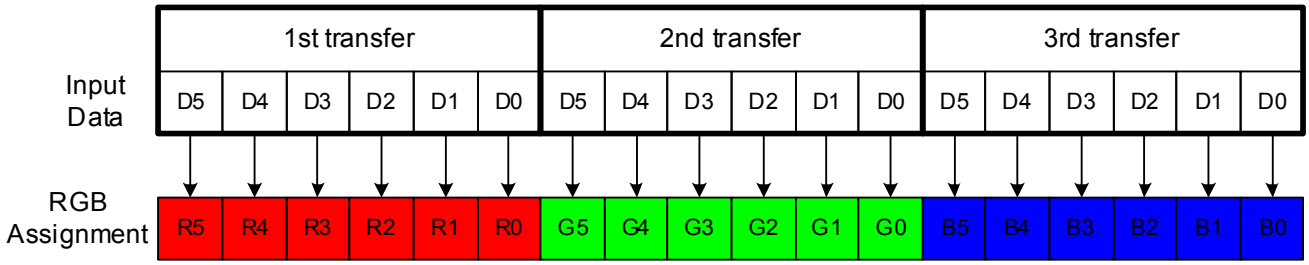
7.6.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



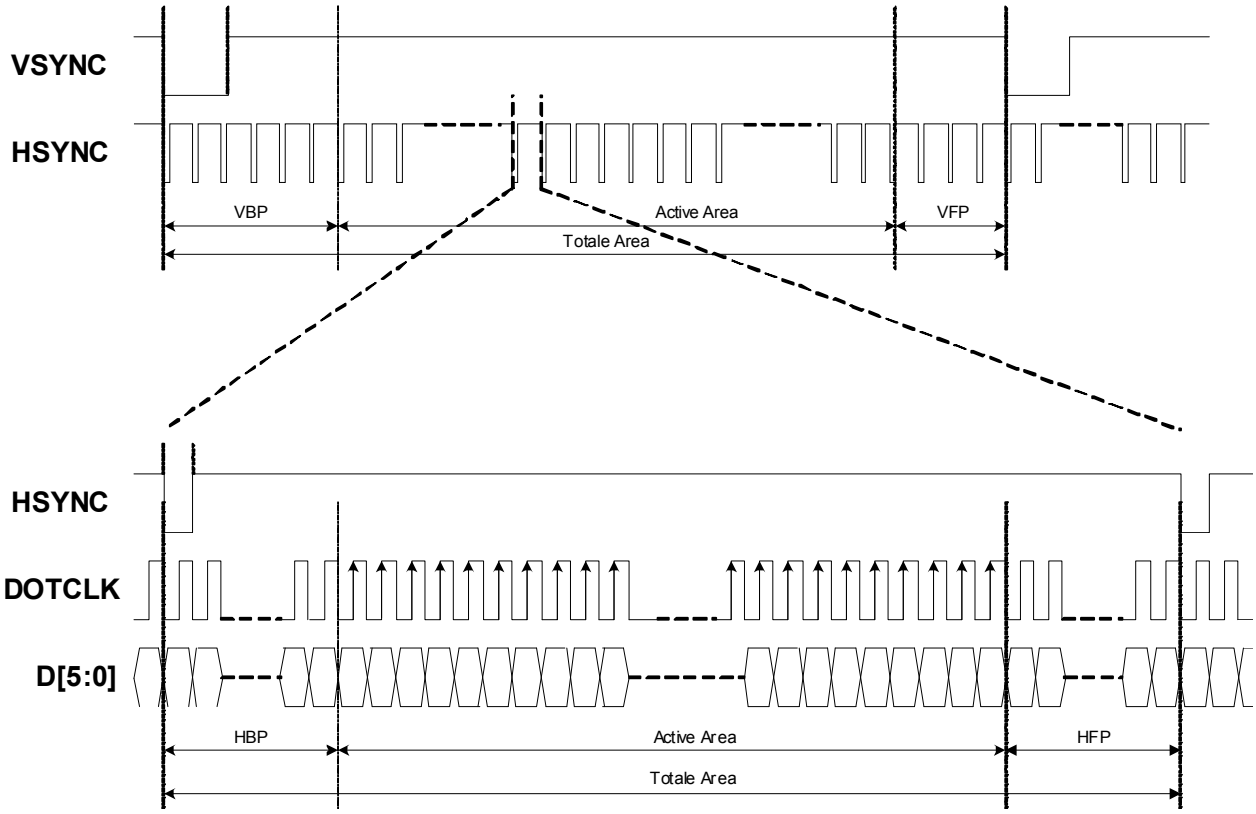
262K color: 18-bit/pixel (RGB 6-6-6 bits input)



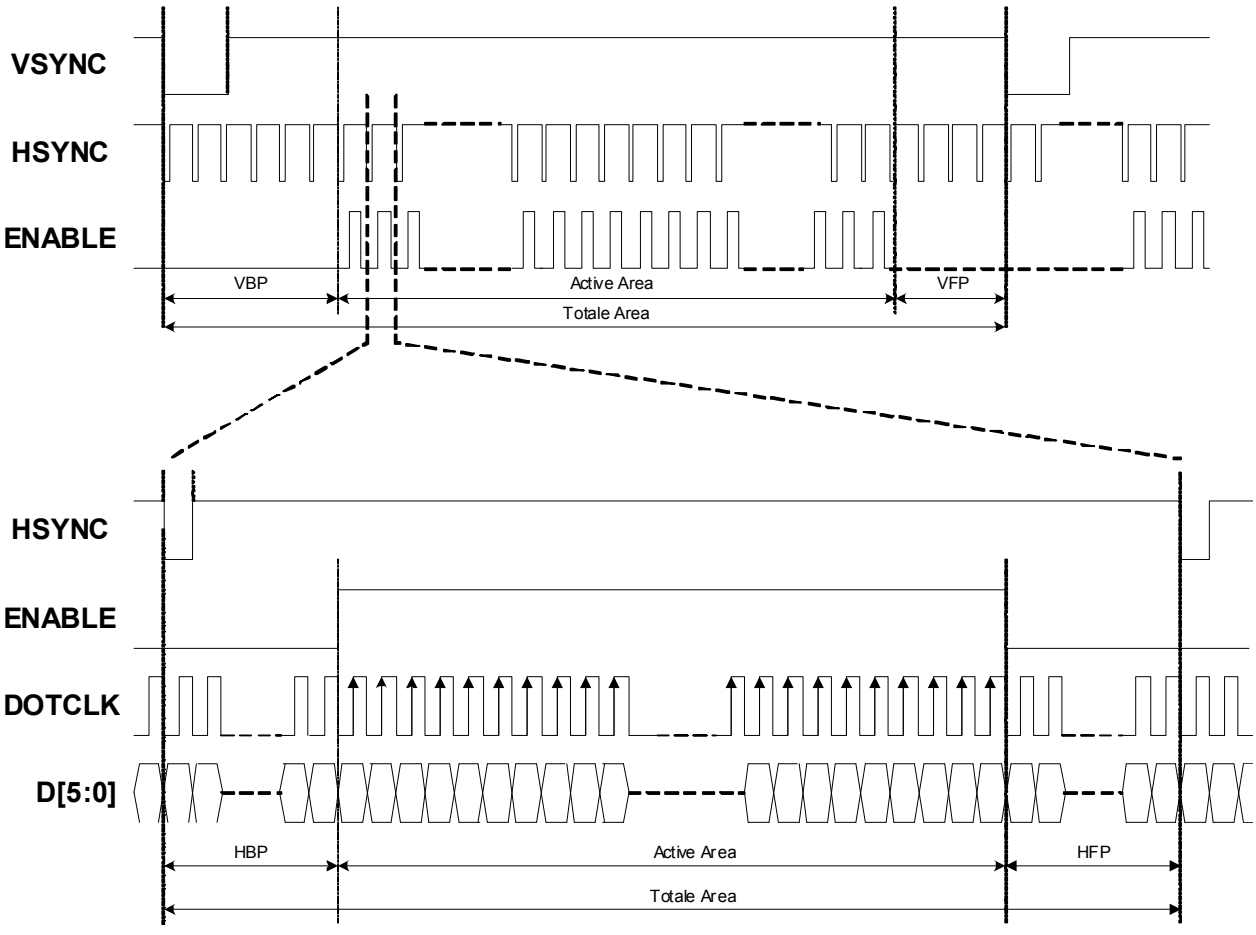
ILI9342 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

SYNC Mode, RCM[1:0]="11"

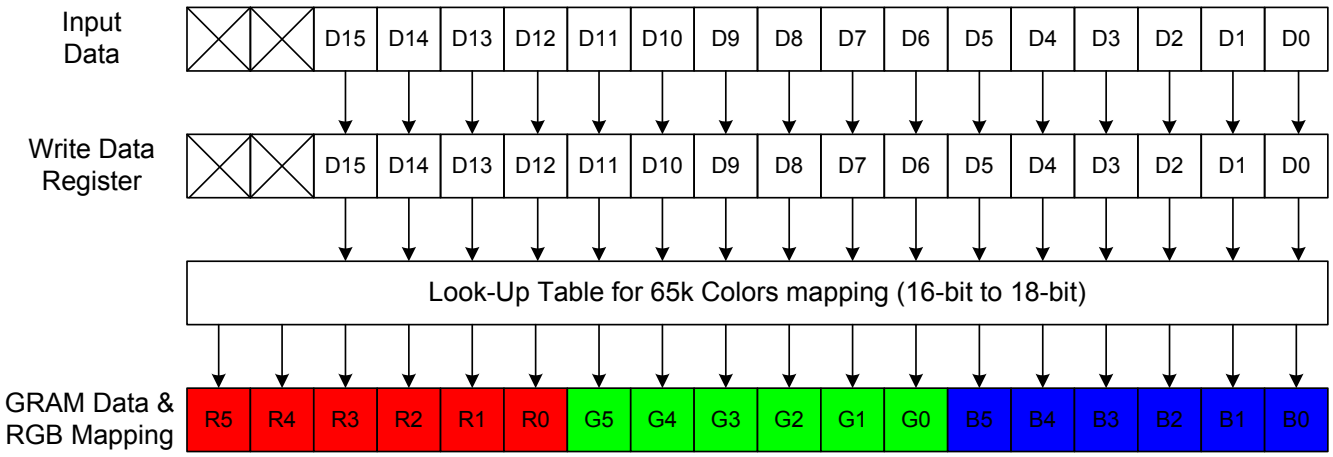


DE Mode, RCM[1:0]="10"



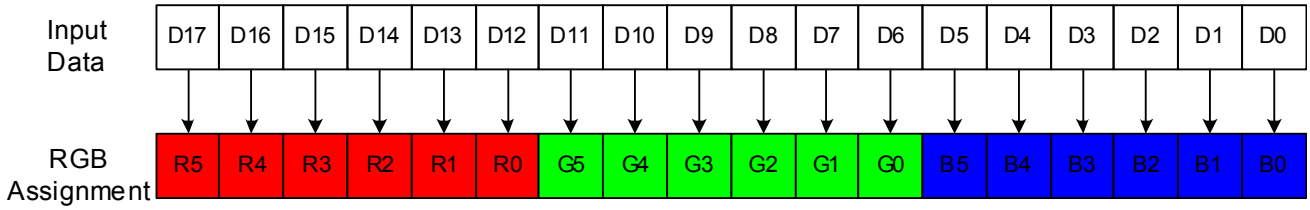
7.6.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [15:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [15:0] according to the VFP/VBP and HFP/HBP settings. The unused D17 and D16 pins must be connected to DGND for ensure normally operation. Registers can be set by the system interface.



7.6.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the system interface.



8. Command

8.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
No Operation	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								XX
	1	↑	1	XX	ID2 [7:0]								XX
	1	↑	1	XX	ID3 [7:0]								XX
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [31:25]							X	00
	1	↑	1	XX	X	D [22:20]			D [19:16]				61
	1	↑	1	XX	X	X	X	X	X	D [10:8]			00
	1	↑	1	XX	D [7:5]			X	X	X	X	X	00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	RIM	DPI [2:0]			X	DBI [2:0]			06
Read Display Image Format	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	D [2:0]			00
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	00
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:6]		X	X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
	1	1	↑	XX	GC [7:0]								01
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC [15:8]								XX
	1	1	↑	XX	SC [7:0]								XX
	1	1	↑	XX	EC [15:8]								XX
	1	1	↑	XX	EC [7:0]								XX
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP [15:8]								XX
	1	1	↑	XX	SP [7:0]								XX
	1	1	↑	XX	EP [15:8]								XX
	1	1	↑	XX	EP [7:0]								XX

Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D [17:0]									XX
Color SET	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh
	1	↑	1	XX	R00 [5:0]								XX
	1	↑	1	XX	Rnn [5:0]								XX
	1	↑	1	XX	R31 [5:0]								XX
	1	↑	1	XX	G00 [5:0]								XX
	1	↑	1	XX	Gnn [5:0]								XX
	1	↑	1	XX	G63 [5:0]								XX
	1	↑	1	XX	B00 [5:0]								XX
	1	↑	1	XX	Bnn [5:0]								XX
	1	↑	1	XX	B31 [5:0]								XX
Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D [17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR [15:8]								00
	1	1	↑	XX	SR [7:0]								00
	1	1	↑	XX	ER [15:8]								00
	1	1	↑	XX	ER [7:0]								EF
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA [15:8]								00
	1	1	↑	XX	TFA [7:0]								00
	1	1	↑	XX	VSA [15:8]								00
	1	1	↑	XX	VSA [7:0]								F0
	1	1	↑	XX	BFA [15:8]								00
	1	1	↑	XX	BFA [7:0]								00
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP [15:8]								00
	1	1	↑	XX	VSP [7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI [2:0]			X	DBI [2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D [17:0]									XX
Read Memory Continue	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D [17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS [8]	00
	1	1	↑	XX	STS [7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	GTS [9:8]		00
	1	↑	1	XX	GTS [7:0]								00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Module's Manufacture [7:0]								XX
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX

	1	↑	1	XX	LCD Module / Driver Version [7:0]								XX
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	BYPASS	RCM [1:0]		X	VSPL	HSPL	DPL	EPL	40
Display Waveform Cycle 1 (In Normal Mode)	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XX	X	X	X	X	X	X	DIVA [1:0]		00
	1	1	↑	XX	X	X	X	RTNA [4:0]					1B
Display Waveform Cycle 2 (In Idle Mode)	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XX	X	X	X	X	X	X	DIVB [1:0]		00
	1	1	↑	XX	X	X	X	RTNB [4:0]					1B
Display Waveform Cycle 3 (In Partial Mode)	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XX	X	X	X	X	X	X	DIVC [1:0]		00
	1	1	↑	XX	X	X	X	RTNC [4:0]					1B
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XX	X	X	X	X	X	NLA	NLB	NLC	02
	1	1	↑	XX	X	X	NW [5:0]						00
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	VFP [6:0]							02
	1	1	↑	XX	0	VBP [6:0]							02
	1	1	↑	XX	0	0	0	HFP [4:0]					0A
	1	1	↑	XX	0	0	0	HBP [4:0]					14
Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	X	X	X	X	PTG [1:0]		PT [1:0]		0A
	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				02
	1	1	↑	XX	X	X	NL [5:0]						1D
	1	1	↑	XX	X	X	PCDIV[5:0]						04
Entry Mode Set	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XX	X	X	X	X	DSTB	GON	DTE	GAS	06
Oscillator Control	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
	1	1	↑	XX	X	X	X	X	FOSC[3:0}				07
Set EXTC	0	1	↑	XX	1	0	1	1	1	0	0	0	B9h
	0	1	↑	XX	EXTC1[7:0]								00
	0	1	↑	XX	EXTC2[7:0]								00
	0	1	↑	XX	EXTC3[7:0]								00
Power Control 1	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XX	X	X	VRH [5:0]						26
	1	1	↑	XX	X	X	X	X	VC [3:0]				09
Power Control 2	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	X	SAP [2:0]			BT [3:0]				10
Power Control 3 (For Normal Mode)	0	1	↑	XX	1	1	0	0	0	0	1	0	C2h
	1	1	↑	XX	X	DCA1 [2:0]			X	DCA0 [2:0]			C2
Power Control 4 (For Idle Mode)	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XX	X	DCB1 [2:0]			X	DCB0 [2:0]			C2
Power Control 5 (For Partial Mode)	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XX	X	DCC1 [2:0]			X	DCC0 [2:0]			C2
VCOM Control 1	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XX	X	VMH [6:0]							31
	1	1	↑	XX	X	VML [6:0]							3C
VCOM Control 2	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
	1	1	↑	XX	nVM	VMF [6:0]							C0
NV Memory Write	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h

	1	1	↑	XX	X	X	X	X	X	PGM_ADR [2:0]					00
	1	1	↑	XX	PGM_DATA [7:0]										XX
NV Memory Protection Key	0	1	↑	XX	1	1	0	1	0	0	0	1			D1h
	1	1	↑	XX	KEY [23:16]										XX
	1	1	↑	XX	KEY [15:8]										XX
	1	1	↑	XX	KEY [7:0]										XX
NV Memory Status Read	0	1	↑	XX	1	1	0	1	0	0	1	0			D2h
	1	↑	1	XX	X	X	X	X	X	X	X	X			XX
	1	↑	1	XX	X	ID2_CNT [2:0]			X	ID1_CNT [2:0]					XX
	1	↑	1	XX	BUSY	VMF_CNT [2:0]			X	ID3_CNT [2:0]					XX
Read ID4	0	↑	1	XX	1	1	0	1	0	0	1	1			D3h
	1	↑	1	XX	X	X	X	X	X	X	X	X			XX
	1	↑	1	XX	0	0	0	0	0	0	0	0			00
	1	↑	1	XX	1	0	0	1	0	0	1	1			93
	1	↑	1	XX	0	1	0	0	0	0	1	0			42
Positive Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	0			E0h
	1	1	↑	XX	X	X	X	x	VP63 [3:0]						XX
	1	1	↑	XX	X	X	VP62 [5:0]								XX
	1	1	↑	XX	X	X	VP61 [5:0]								XX
	1	1	↑	XX	X	X	X	X	VP59 [3:0]						XX
	1	1	↑	XX	X	X	X	VP57 [4:0]							XX
	1	1	↑	XX	X	X	X	X	VP50 [3:0]						XX
	1	1	↑	XX	X	VP20 [6:0]									XX
	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]						XX
	1	1	↑	XX	X	VP20 [6:0]									XX
	1	1	↑	XX	X	X	X	X	VP13[3:0]						XX
	1	1	↑	XX	X	X	X	VP6 [4:0]							XX
	1	1	↑	XX	X	X	X	X	VP4 [3:0]						XX
	1	1	↑	XX	X	X	VP2 [5:0]								XX
	1	1	↑	XX	X	X	VP1 [5:0]								XX
	1	1	↑	XX	X	X	X	X	VP0 [3:0]						XX
Negative Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	1			E1h
	1	1	↑	XX	X	X	X	X	VN63 [3:0]						00
	1	1	↑	XX	X	X	VN62 [5:0]								23
	1	1	↑	XX	X	X	VN61 [5:0]								26
	1	1	↑	XX	X	X	X	X	VN59 [3:0]						05
	1	1	↑	XX	X	X	X	VN57 [4:0]							10
	1	1	↑	XX	X	X	X	X	VN50 [3:0]						04
	1	1	↑	XX	X	VN43 [6:0]									39
	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]						24
	1	1	↑	XX	X	VN20 [6:0]									4B
	1	1	↑	XX	X	X	X	X	VN13 [3:0]						03
	1	1	↑	XX	X	X	X	VN6 [4:0]							0B
	1	1	↑	XX	X	X	X	X	VN4 [3:0]						0B
	1	1	↑	XX	X	X	VN2 [5:0]								33
	1	1	↑	XX	X	X	VN1 [5:0]								37
	1	1	↑	XX	X	X	X	x	VN0 [3:0]						0F
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0			E2h
	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]						XX
	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]						XX
	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]						XX
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1			E3h
	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]						XX
	1	1	↑	XX	RFAx [3:0]				BFAx [3:0]						XX
	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]						XX
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0			F6h

	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	X	BGR_EOR	X	X	WEMODE	01
	1	1	↑	XX	X	X	EPF [1:0]		X	X	X	X	00
	1	1	↑	XX	X	X	ENDIAN	X	DM [1:0]		RM	RIM	00
Get GPIO0~7 Status	0	1	↑	XX	1	1	1	1	0	1	1	1	F7h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	GPI [7:0]								00
Set GPIO0~7 Status	0	1	↑	XX	1	1	1	1	1	0	0	0	F8h
	0	1	↑	XX	GPO[7:0]								00
	0	1	↑	XX							IE	OEB	00

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP (00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9342 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.

8.2. Description of Regulative Command Set

8.2.1. NOP (00h)

<table>
<tr><th>00h</th><th colspan="13">NOP (No Operation)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter.</td></tr>
<tr><td>Description</td><td colspan="13">This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">None</td></tr>
</table>

8.2.2. Software Reset (01h)

01h	SWRESET												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Parameter	No Parameter.												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command X = Don't care.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												

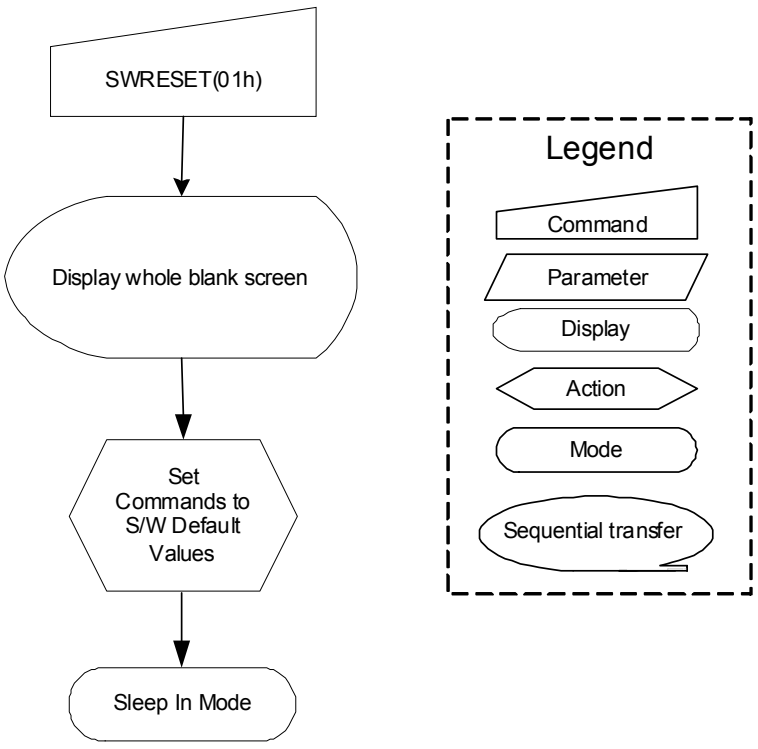
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart



8.2.3. Read display identification information (04h)

04h	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	ID1 [7:0]								XX
3rd Parameter	1	↑	1	XX	ID2 [7:0]								XX
4th Parameter	1	↑	1	XX	ID3 [7:0]								XX
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2 [7:0]): LCD module/driver version ID. The 4th parameter (ID3 [7:0]): LCD module/driver ID.												
Restriction													

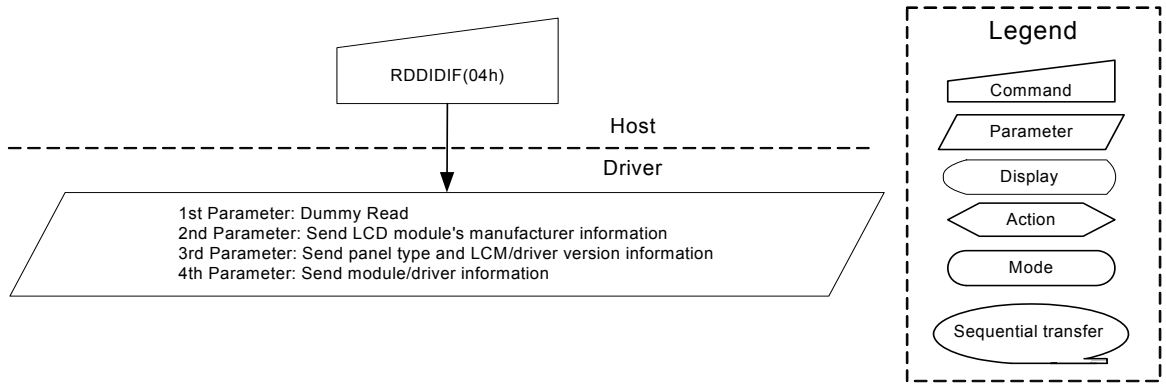
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description

Flow Chart



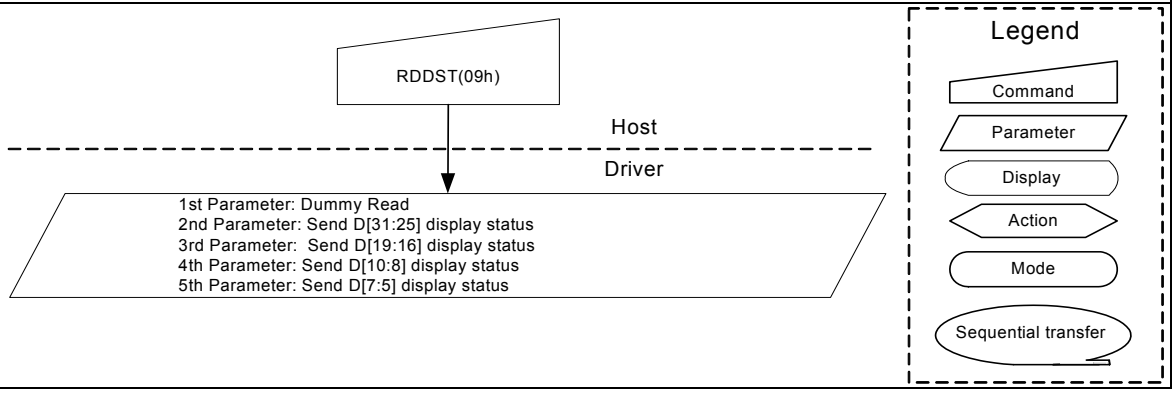
8.2.4. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D [31:25]							0	00
3rd Parameter	1	↑	1	XX	0	D [22:20]			D [19:16]				61
4th Parameter	1	↑	1	XX	D15	0	D13	0	0	D [10:8]			00
5th Parameter	1	↑	1	XX	D [7:5]			0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster OFF
		1	Booster ON
D30	Row address order	0	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	0	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	0	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL B4='0')
		1	LCD Refresh Bottom to Top (When MADCTL B4='1').
D26	RGB/BGR order	0	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	0	---
D23	Not used	0	---
D22	Interface color pixel format definition	011	12-bit/pixel
D21		101	16-bit/pixel
D20		110	18-bit/pixel
D19	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON.
D17	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode.
D16	Display normal mode ON/OFF	0	Display Normal Mode OFF.
		1	Display Normal Mode ON.
D15	Vertical scrolling status	0	Vertical Scroll OFF
		1	Vertical Scroll ON
D14	Not used	0	---
D13	Inversion status	0	Inversion OFF
		1	Inversion ON
D12	All pixel ON	0	Not defined
D11	All pixel OFF	0	Not defined
D10	Display ON/OFF	0	Display is OFF
		1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON
D[8:6]	Gamma curve selection	000	GC0
		001	GC1
		010	GC2
		011	GC3
		other	Not defined

<table>
<tr><td></td><td>
<table>
<tr><td rowspan="2">D5</td><td rowspan="2">Tearing effect line mode</td><td>0</td><td>Mode 1, V-Blanking only</td></tr>
<tr><td>1</td><td>Mode 2, both H-Blanking and V-Blanking.</td></tr>
<tr><td>D4</td><td>Not used</td><td>0</td><td>---</td></tr>
<tr><td>D3</td><td>Not used</td><td>0</td><td>---</td></tr>
<tr><td>D2</td><td>Not used</td><td>0</td><td>---</td></tr>
<tr><td>D1</td><td>Not used</td><td>0</td><td>---</td></tr>
<tr><td>D0</td><td>Not used</td><td>0</td><td>---</td></tr>
</table>
X = Don’t care
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>32’h00610000h</td></tr>
<tr><td>SW Reset</td><td>32’h00610000h</td></tr>
<tr><td>HW Reset</td><td>32’h00610000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

8.2.5. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	08

Description

This command indicates the current status of the display as described in the table below::

Bit	Value	Description	Comment
D7	0	Booster Off or has a fault.	---
	1	Booster On and working OK	---
D6	0	Idle Mode Off.	---
	1	Idle Mode On.	---
D5	0	Partial Mode Off.	---
	1	Partial Mode On.	---
D4	0	Sleep In Mode	---
	1	Sleep Out Mode	---
D3	0	Display Normal Mode Off.	---
	1	Display Normal Mode On	---
D2	0	Display is Off.	---
	1	Display is On	---
D1	--	Not Defined	Set to '0'
D0	--	Not Defined	Set to '0'

X = Don't care

Restriction

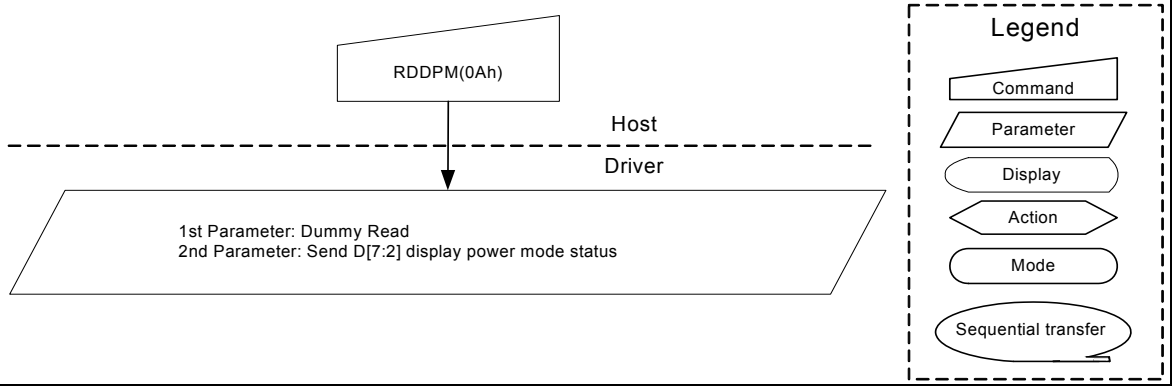
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h08h
SW Reset	8'h08h
HW Reset	8'h08h

Flow Chart



8.2.6. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description	Comment
D7	0	Top to Bottom (When MADCTL B7='0').	---
	1	Bottom to Top (When MADCTL B7='1').	---
D6	0	Left to Right (When MADCTL B6='0')	---
	1	Right to Left (When MADCTL B6='1')	---
D5	0	Normal Mode (When MADCTL B5='0').	---
	1	Reverse Mode (When MADCTL B5='1')	---
D4	0	LCD Refresh Top to Bottom (When MADCTL B4='0')	---
	1	LCD Refresh Bottom to Top (When MADCTL B4='1').	---
D3	0	RGB (When MADCTL B3='0')	---
	1	BGR (When MADCTL B3='1').	---
D2	0	LCD Refresh Left to Right (When MADCTL B2='0').	---
	1	LCD Refresh Right to Left (When MADCTL B2='1').	---
D1	--	Switching between Segment outputs and RAM	Set to '0'
D0	--	Switching between Segment outputs and RAM	Set to '0'

X = Don't care

Restriction

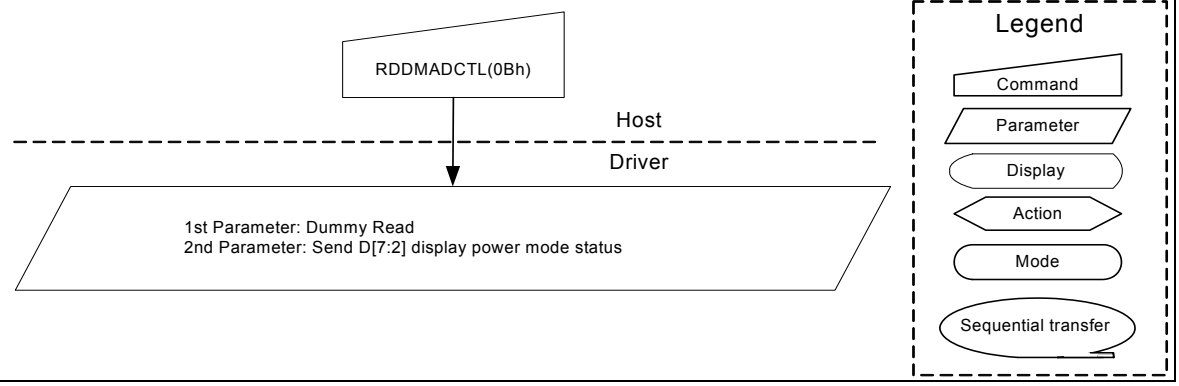
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No Change
HW Reset	8'h00h

Flow Chart



8.2.7. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display COLMOD)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	RIM	DPI [2:0]			0	DBI [2:0]			06

Description

This command indicates the current status of the display as described in the table below:

RIM	DPI[2:0]			RGB Interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	12 bits / pixel
0	1	0	0	Reserved
0	1	0	1	16 bits / pixel
0	1	1	0	18 bits / pixel
0	1	1	1	Reserved
1	1	0	1	16 bits / pixel (6-bit 3 times data transfer)
1	1	1	0	18 bits / pixel (6-bit 3 times data transfer)

DBI [2:0]			MPU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	12 bits / pixel
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

X = Don't care

Restriction

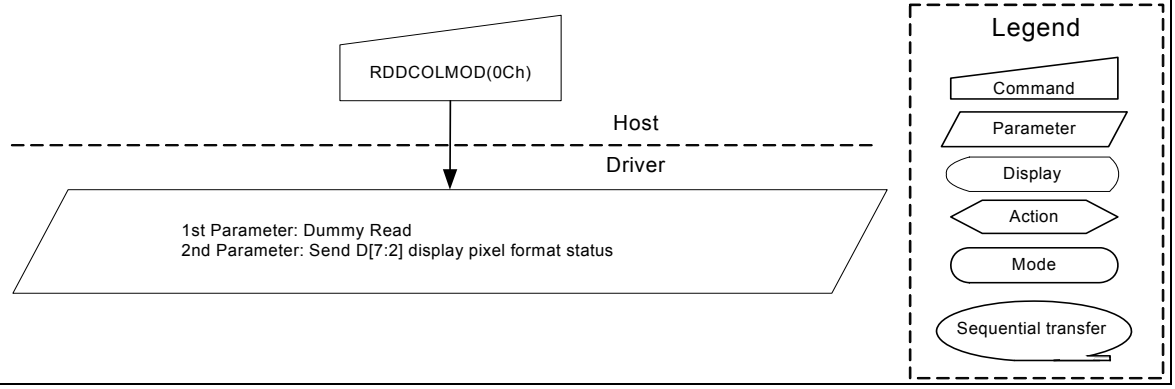
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	RIM	DPI [2:0]	DBI [2:0]
Power On Sequence	1'b0	3'b000	3'b110
SW Reset	No Chang	No Chang	No Chang
HW Reset	1'b0	3'b000	3'b110

Flow Chart



8.2.8. Read Display Image Format (0Dh)

0Dh	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	0	0	0	0	0	D [2:0]			00

Description

This command indicates the current status of the display as described in the table below:

D [2:0]	Description
000	Gamma curve 1 (GC0 G2.2)
001	Gamma curve 2 (GC1 G1.8)
010	Gamma curve 3 (GC2 G2.5)
011	Gamma curve 4 (GC3 G1.0)
Other	Not defined

X = Don't care

Restriction

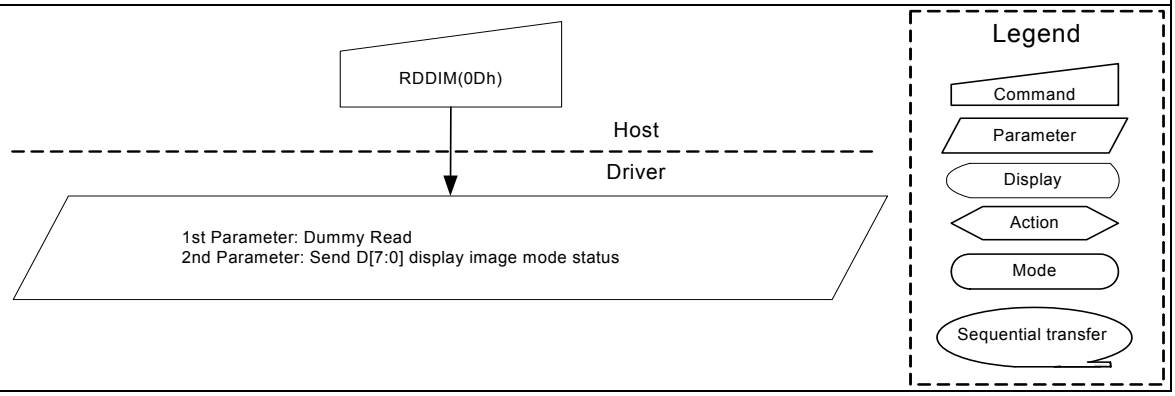
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3'b000
SW Reset	3'b000
HW Reset	3'b000

Flow Chart



8.2.9. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description
D7	0	Tearing effect line OFF
	1	Tearing effect line ON
D6	0	Tearing effect line mode 1
	1	Tearing effect line mode 2
D5	0	Horizontal sync. (RGB interface) OFF
	1	Horizontal sync. (RGB interface) ON
D4	0	Vertical sync. (RGB interface) OFF
	1	Vertical sync. (RGB interface) ON
D3	0	Pixel clock (DOTCLK, RGB interface) OFF
	1	Pixel clock (DOTCLK, RGB interface) ON
D2	0	Data enable (DE, RGB interface) OFF
	1	Data enable (DE, RGB interface) ON
D1	0	Reserved
D0	0	Reserved

X = Don't care

Restriction

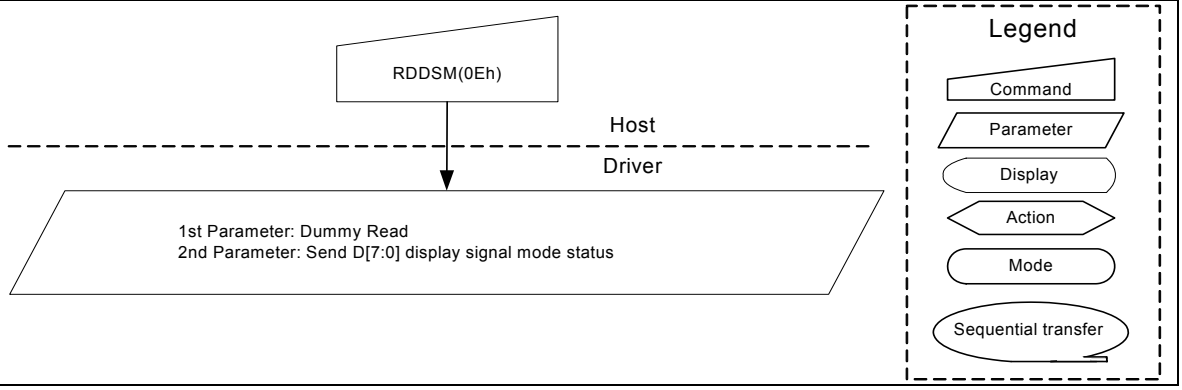
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00

Description

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

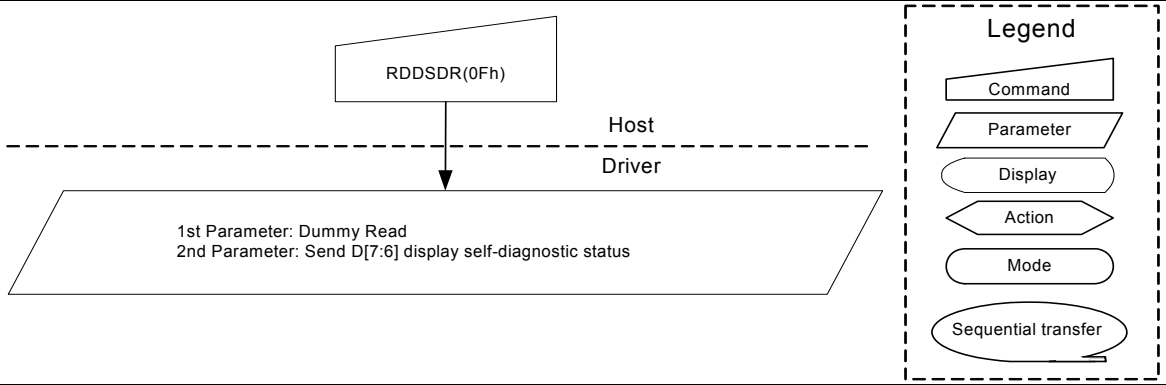
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart

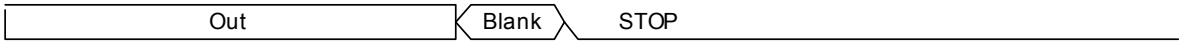


8.2.11. Enter Sleep Mode (10h)

10h	SPLIN (Enter Sleep Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter												

Description

This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.



MPU interface and memory are still working and the memory keeps its contents.

X = Don't care

Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

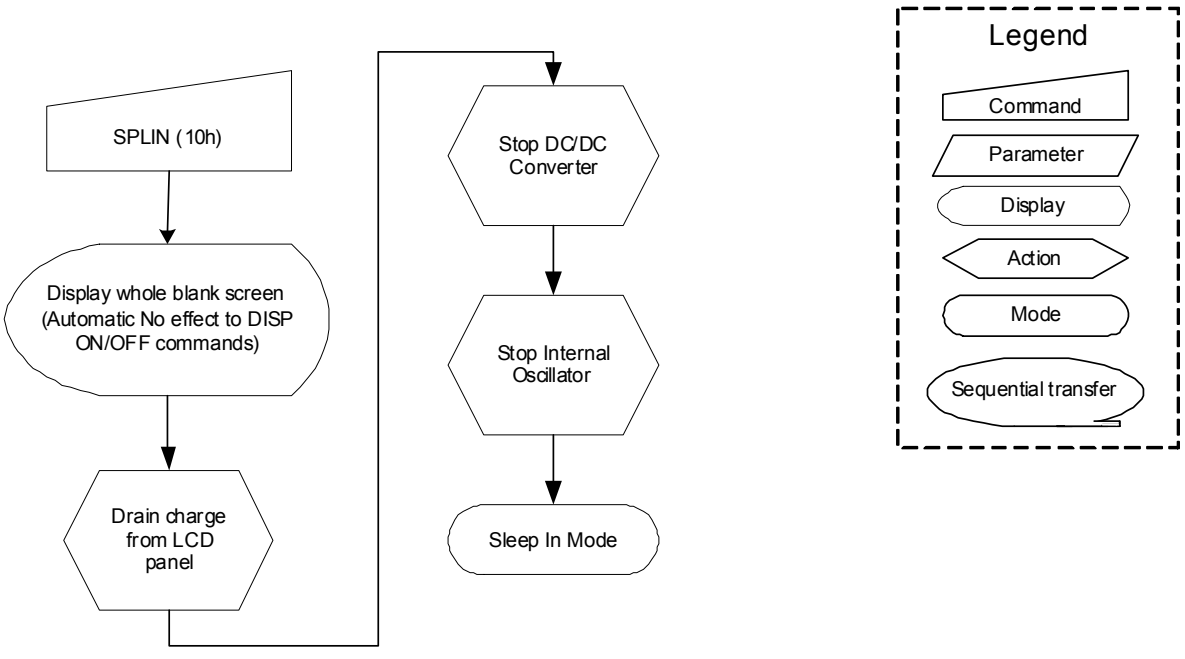
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

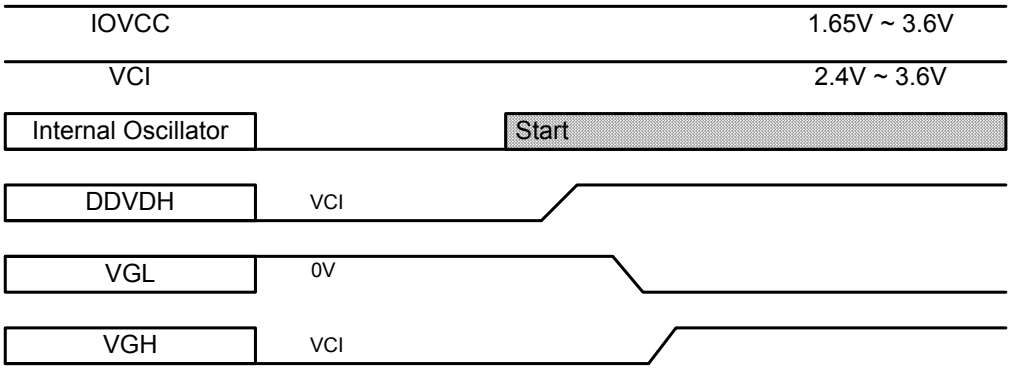
Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



8.2.12. Sleep Out (11h)

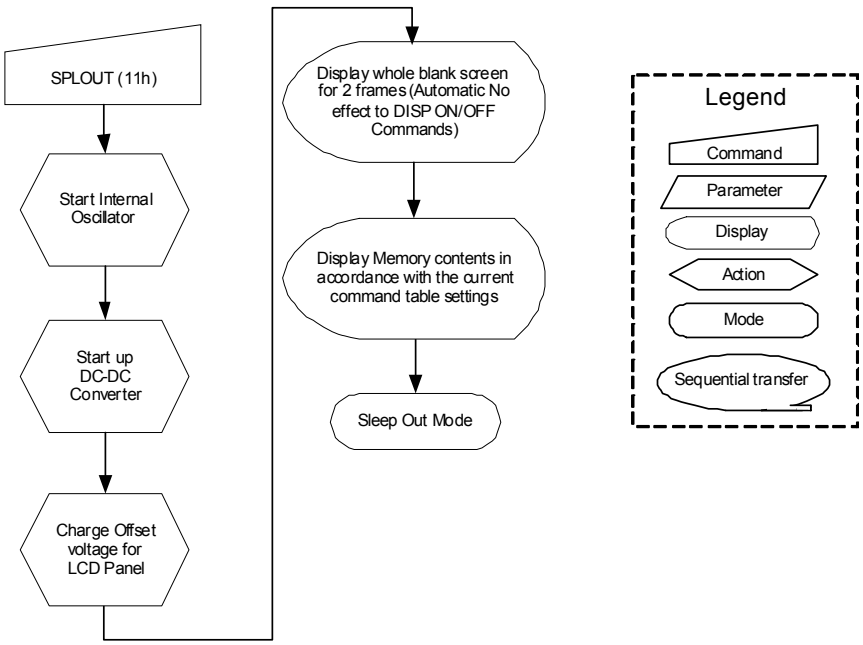
11h	SLPOUT (Sleep Out)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Parameter	No Parameter												
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  X = Don't care											
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the clock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this 120msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued.



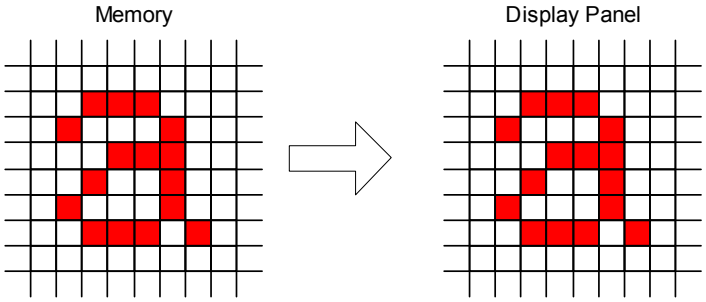
8.2.13. Partial Mode ON (12h)

<table>
<tr><th>12h</th><th colspan="12">PTLON (Partial Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

8.2.14. Normal Display Mode ON (13h)

<table>
<tr><th>13h</th><th colspan="13">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

8.2.15. Display Inversion OFF (20h)

20h	DINVOFF (Display Inversion OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status.  X = Don't care												
Restriction	This command has no effect when module already is inversion OFF mode.												

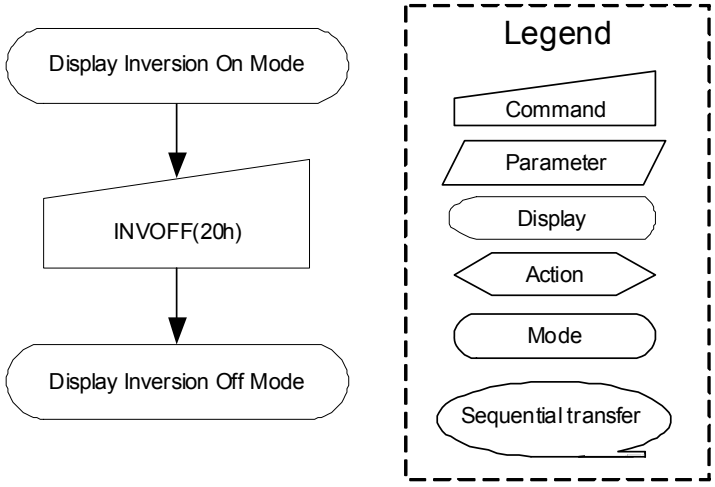
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

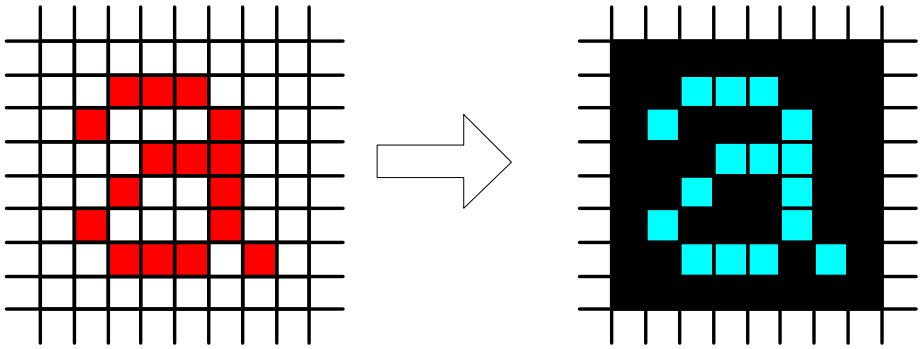
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.16. Display Inversion ON (21h)

21h	DINVON (Display Inversion ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written.  X = Don't care												
Restriction	This command has no effect when module already is inversion ON mode.												

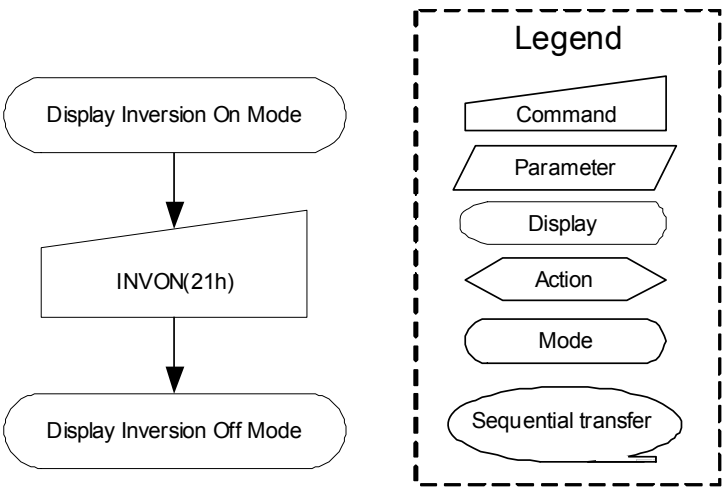
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.17. Gamma Set (26h)

26h	GAMSET (Gamma Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
Parameter	1	1	↑	XX	GC [7:0]								01

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC [7:0]	Curve Selected
01h	Gamma curve 1 (G2.2)
02h	Gamma curve 2 (G1.8)
04h	Gamma curve 3 (G2.5)
08h	Gamma curve 4 (G1.0)

Note: All other values are undefined.

X = Don't care

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

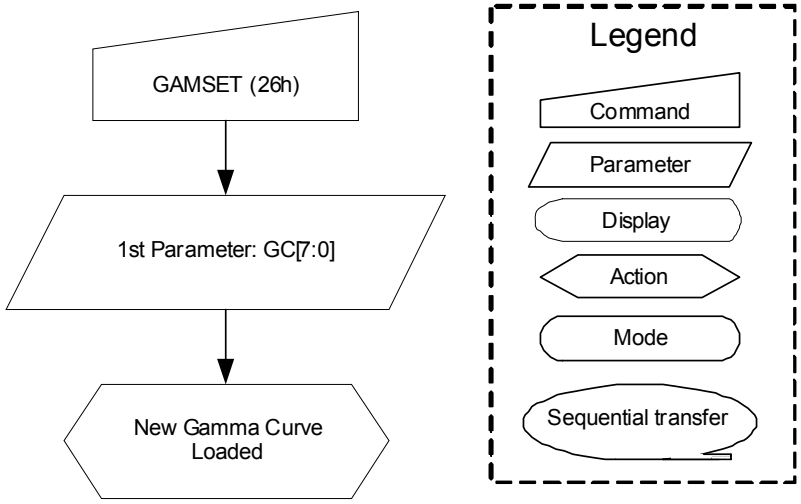
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

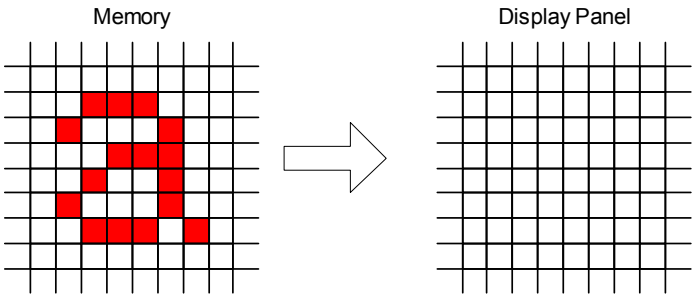
Default

Status	Default Value
Power On Sequence	8'h01h
SW Reset	8'h01h
HW Reset	8'h01h

Flow Chart



8.2.18. Display OFF (28h)

28h	DISPOFF (Display OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = Don't care.												
Restriction	This command has no effect when module is already in display off mode.												

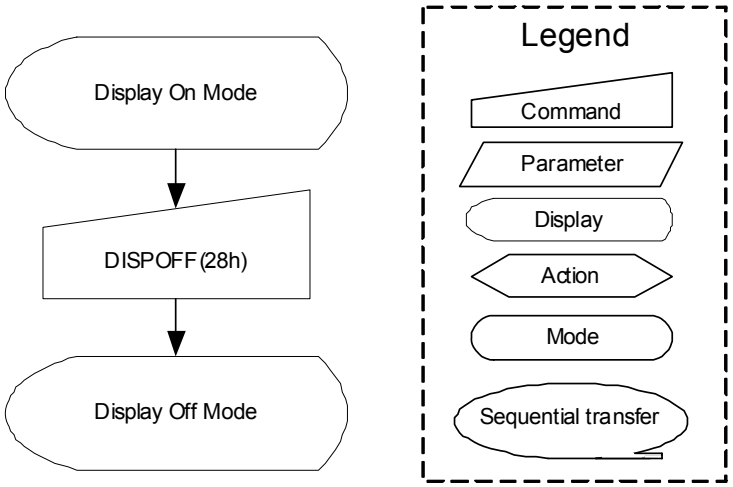
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

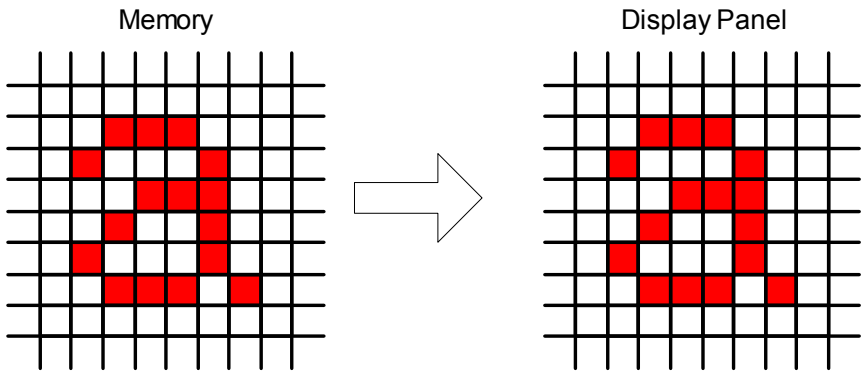
Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



8.2.19. Display ON (29h)

29h	DISPON (Display ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status  X = Don't care.												
Restriction	This command has no effect when module is already in display on mode.												

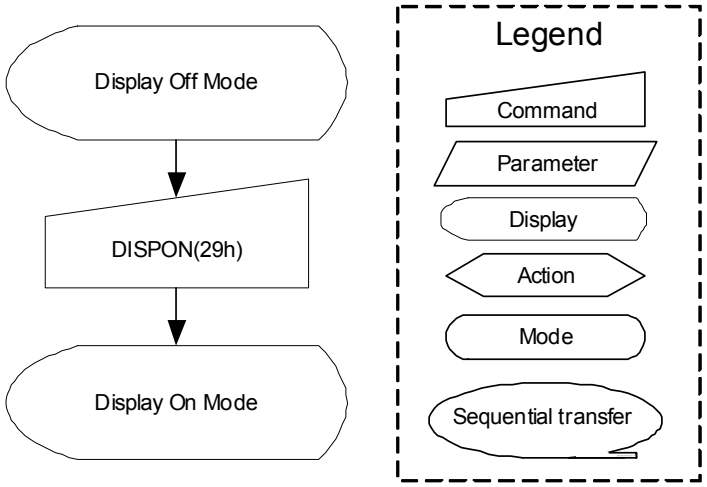
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

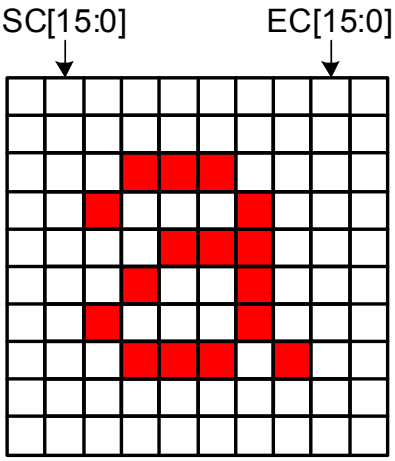


8.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2ndParameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MPU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



X = Don't care

Restriction

SC [15:0] always must be equal to or less than EC [15:0].

Note 1: When SC [15:0] or EC [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 = 1), data of out of range will be ignored

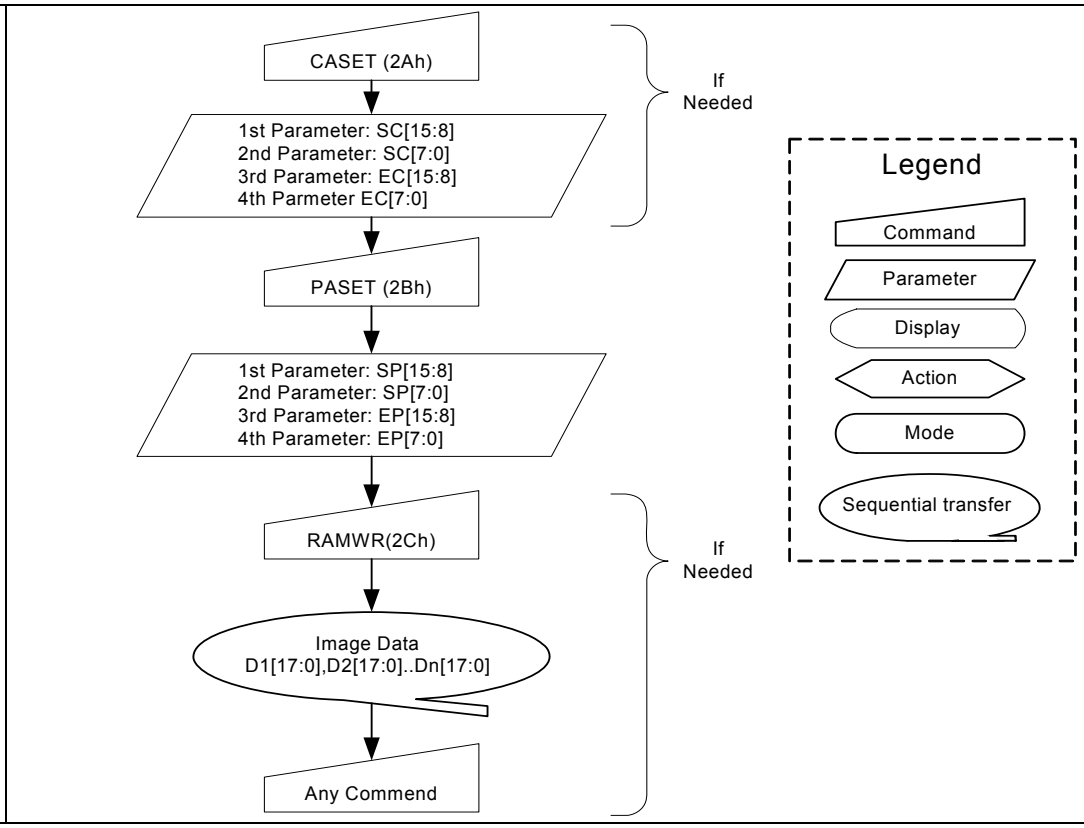
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC [15:0]=0000h	EC [15:0]=013Fh
SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=013Fh If MADCTL's B5 = 1: EC [15:0]=00EFh
HW Reset	SC [15:0]=0000h	EC [15:0]=013Fh

Flow Chart

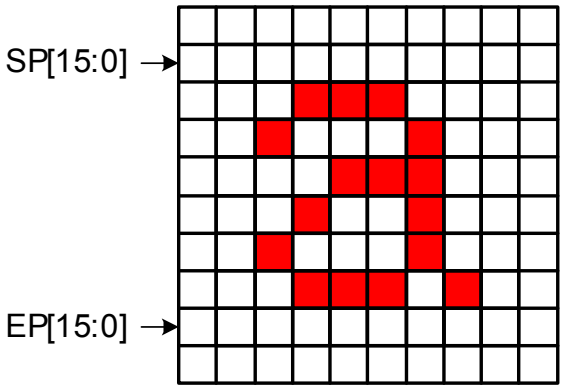


8.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
2ndParameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rdParameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MPU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



X = Don't care

Restriction

SP [15:0] always must be equal to or less than EP [15:0]

Note 1: When SP [15:0] or EP [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored.

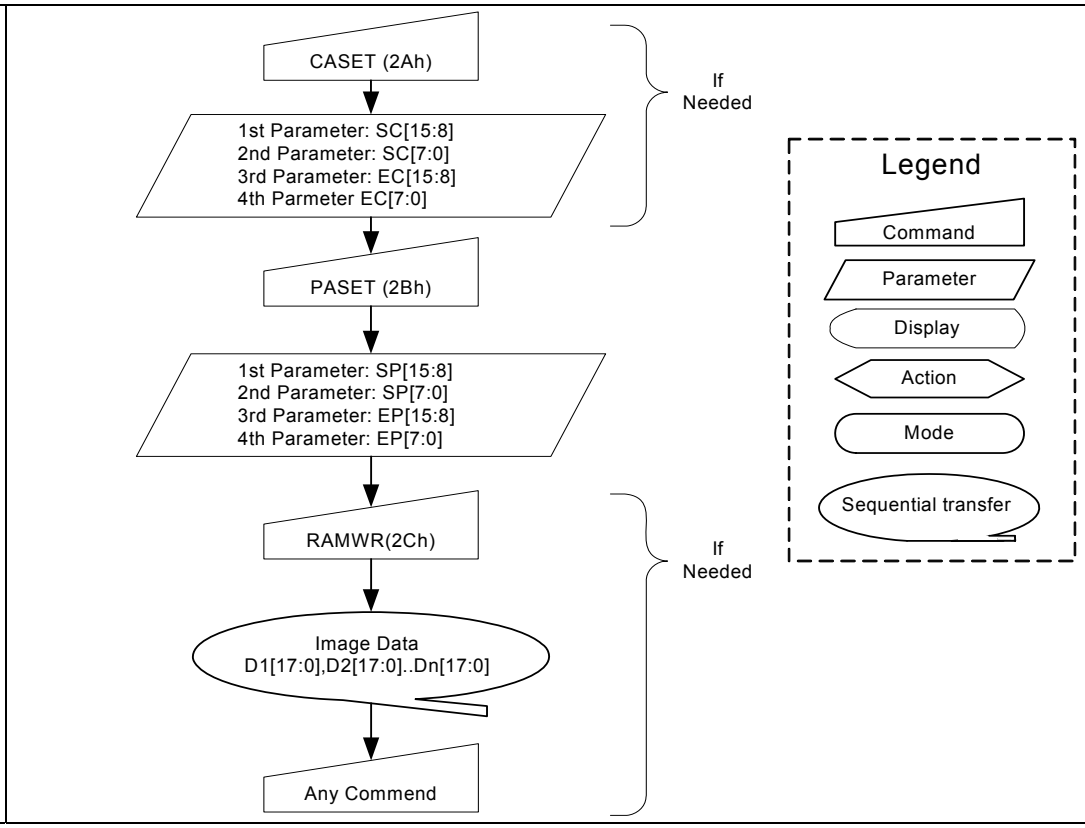
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=00EFh
SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=00EFh If MADCTL's B5 = 1: EP [15:0]=013Fh
HW Reset	SP [15:0]=0000h	EP [15:0]=00EFh

Flow Chart



8.2.22. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
Nth Parameter	1	1	↑	Dn [17:0]									XX
Description	This command is used to transfer data from MPU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.												
Restriction	In all color modes, there is no restriction on length of parameters.												

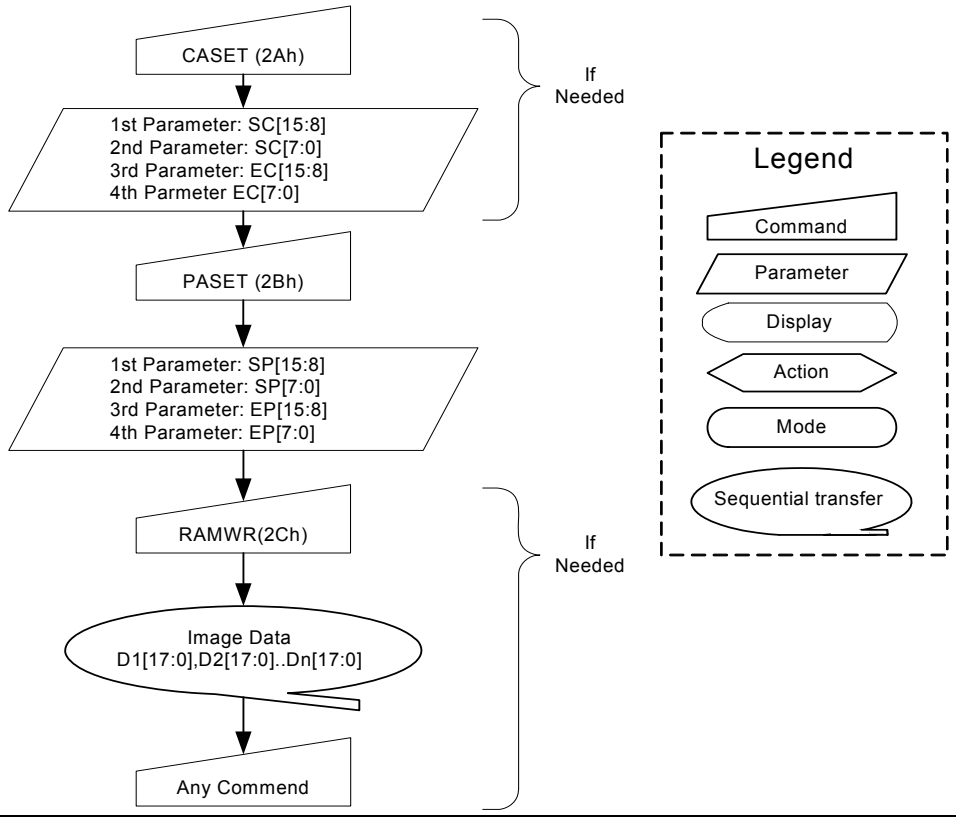
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



8.2.23. Color Set (2Dh)

2Dh	RGBSET (Color Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh
1st Parameter	1	1	↑	XX	R00 [5:0]								XX
nth Parameter	1	1	↑	XX	Rnn [5:0]								XX
32ndParameter	1	1	↑	XX	R31 [5:0]								XX
33rdParameter	1	1	↑	XX	G00 [5:0]								XX
nth Parameter	1	1	↑	XX	Gnn [5:0]								XX
96thParameter	1	1	↑	XX	G64 [5:0]								XX
97thParameter	1	1	↑	XX	B00 [5:0]								XX
nth Parameter	1	1	↑	XX	Bnn [5:0]								XX
128thParameter	1	1	↑	XX	B31 [5:0]								XX

Description

This command is used to define the LUT for 16-bit to 18-bit color depth conversion.

128 bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.4 are referred.

This command has no effect on other commands, parameter and contents of frame memory. Visible change takes effect next time the frame memory is written to.

Restriction

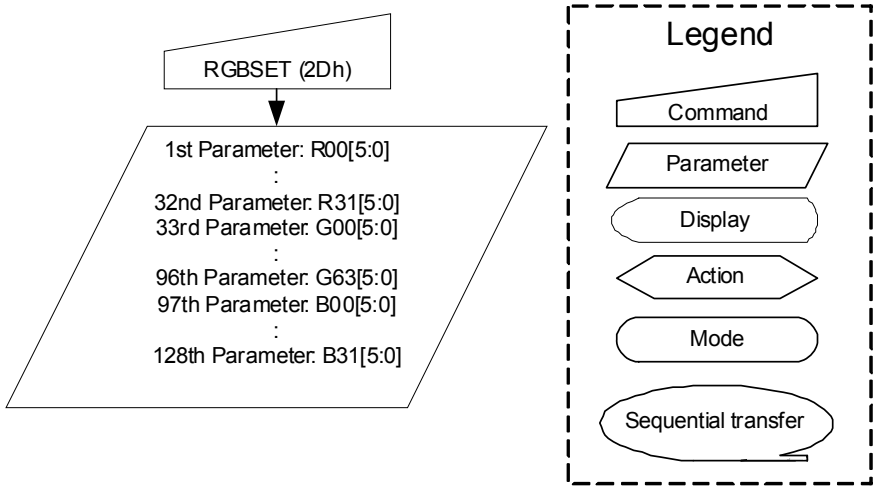
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random values
SW Reset	Contents of LUT protected
HW Reset	Random values

Flow Chart



8.2.24. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
(N+1)th Parameter	1	1	↑	Dn [17:0]									XX

Description

This command transfers image data from ILI9342's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If Memory Access control B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

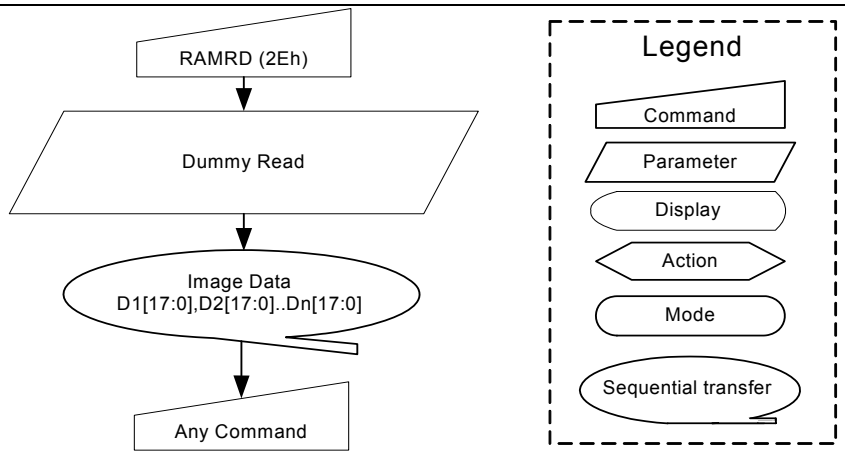
There is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

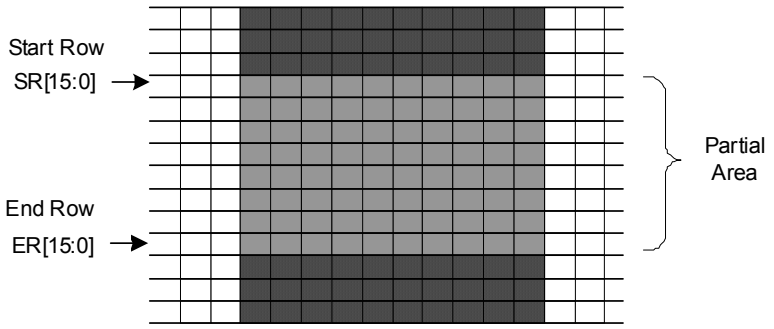
8.2.25. Partial Area (30h)

30h	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2ndParameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rdParameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	00
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EF

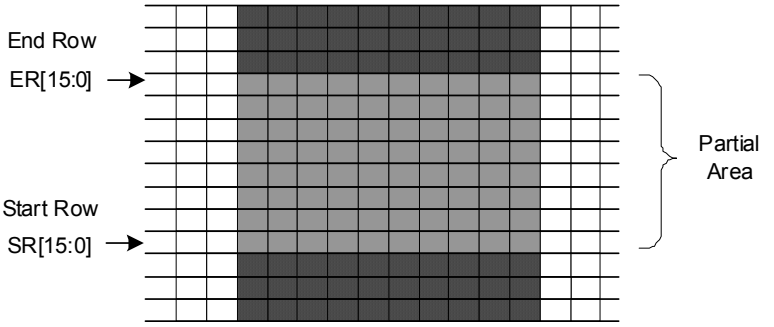
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

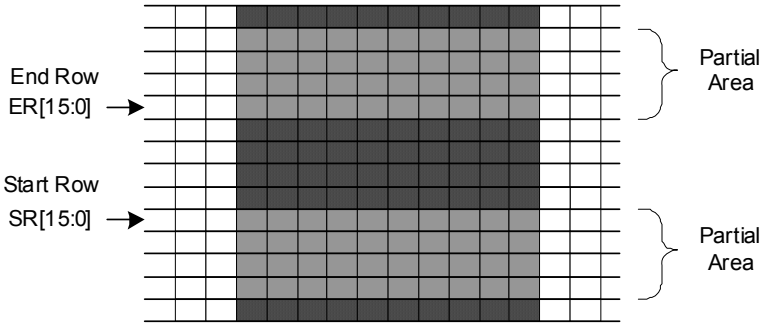
If End Row>Start Row when MADCTL B4=0:-



If End Row>Start Row when MADCTL B4=1:-



If End Row<Start Row when MADCTL B4=0:-



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 00EFh.

Register Availability

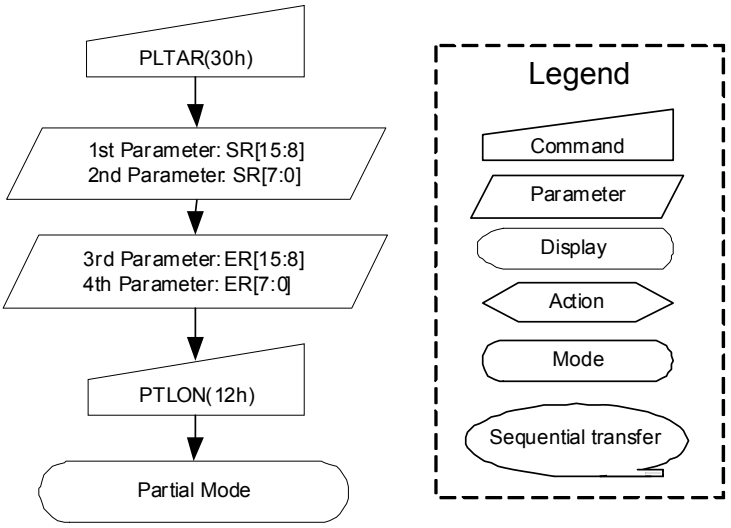
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

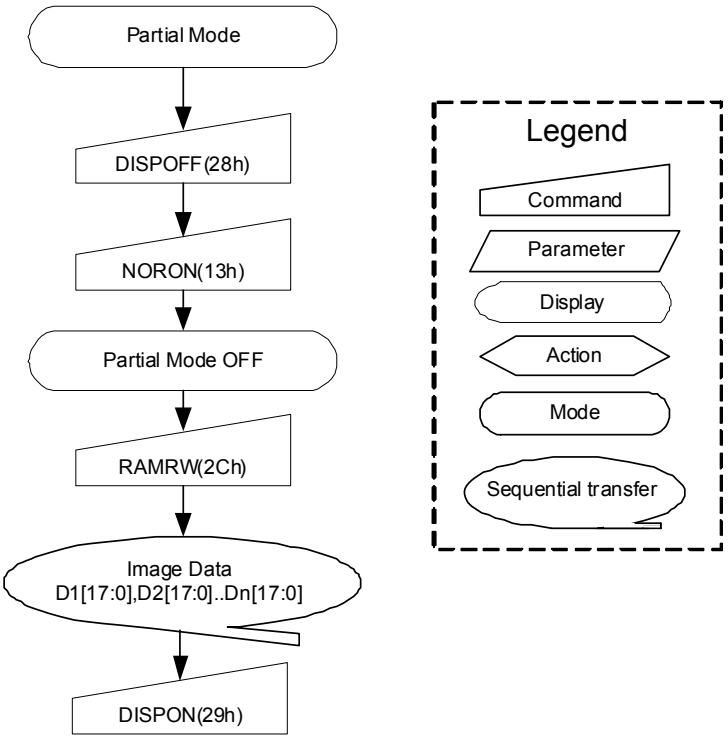
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h00EFh
SW Reset	16'h 0000h	16'h 00EFh
HW Reset	16'h 0000h	16'h 00EFh

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



8.2.26. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	↑	1	XX	TFA [15:8]								00
2nd Parameter	1	↑	1	XX	TFA [7:0]								00
3rd Parameter	1	↑	1	XX	VSA [15:8]								00
4th Parameter	1	↑	1	XX	VSA [7:0]								F0
5th Parameter	1	↑	1	XX	BFA [15:8]								00
6th Parameter	1	↑	1	XX	BFA [7:0]								00

Description

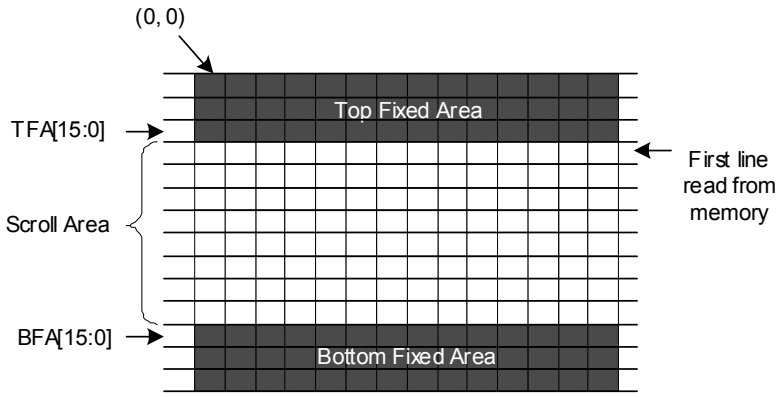
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.

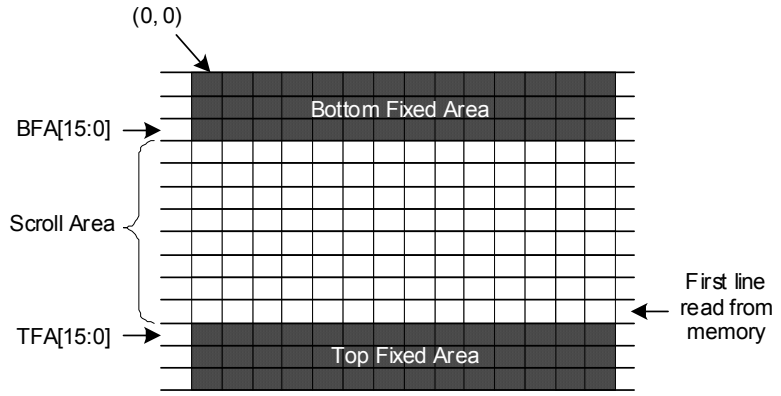


When MADCTL B4=1

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



X = Don't care

Restriction

Register Availability

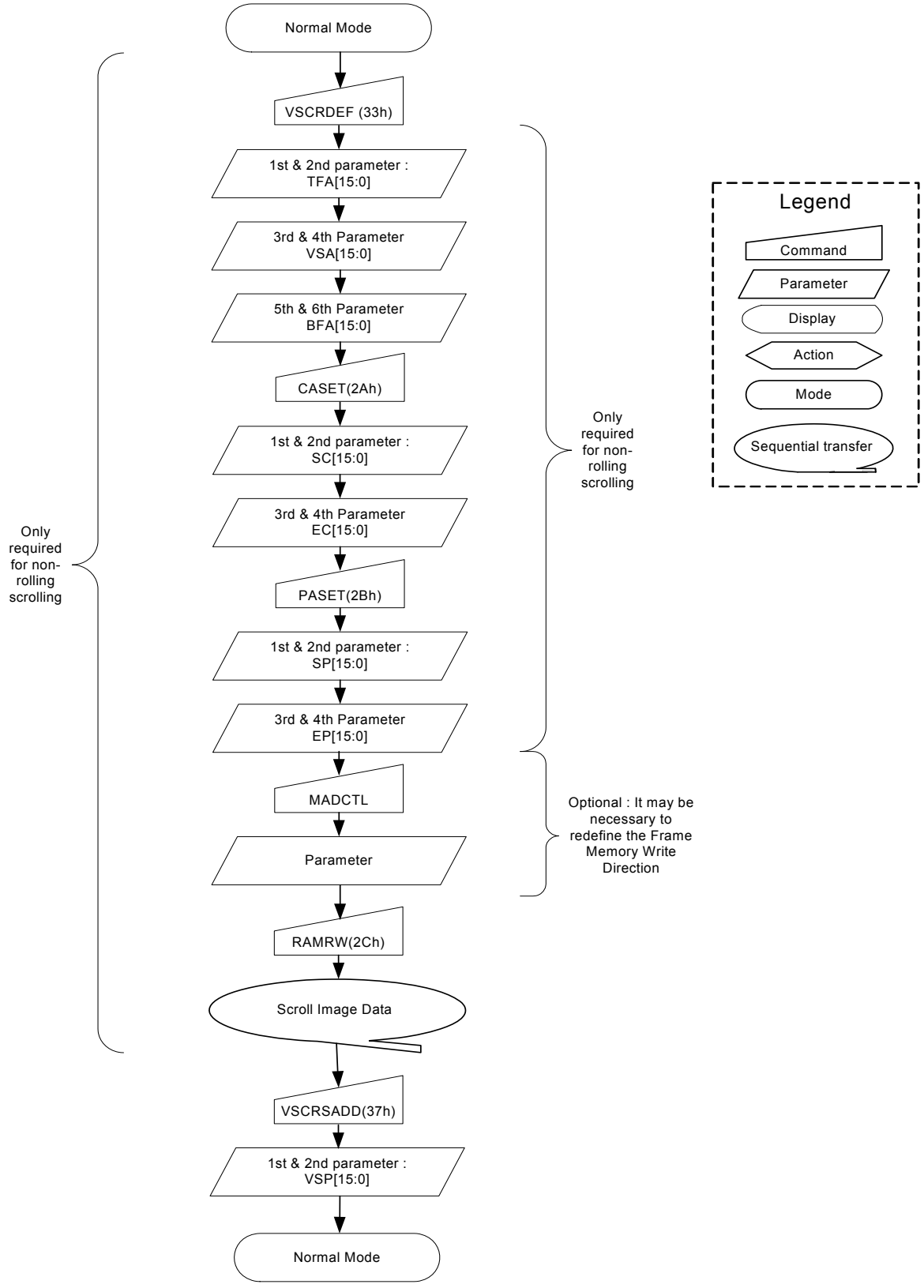
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TFA [15:0]	VSA [15:0]	BFA [15:0]
Power On Sequence	16'h0000h	16'h00EFh	16'h0000h
SW Reset	16'h0000h	16'h00EFh	16'h0000h
HW Reset	16'h0000h	16'h00EFh	16'h0000h

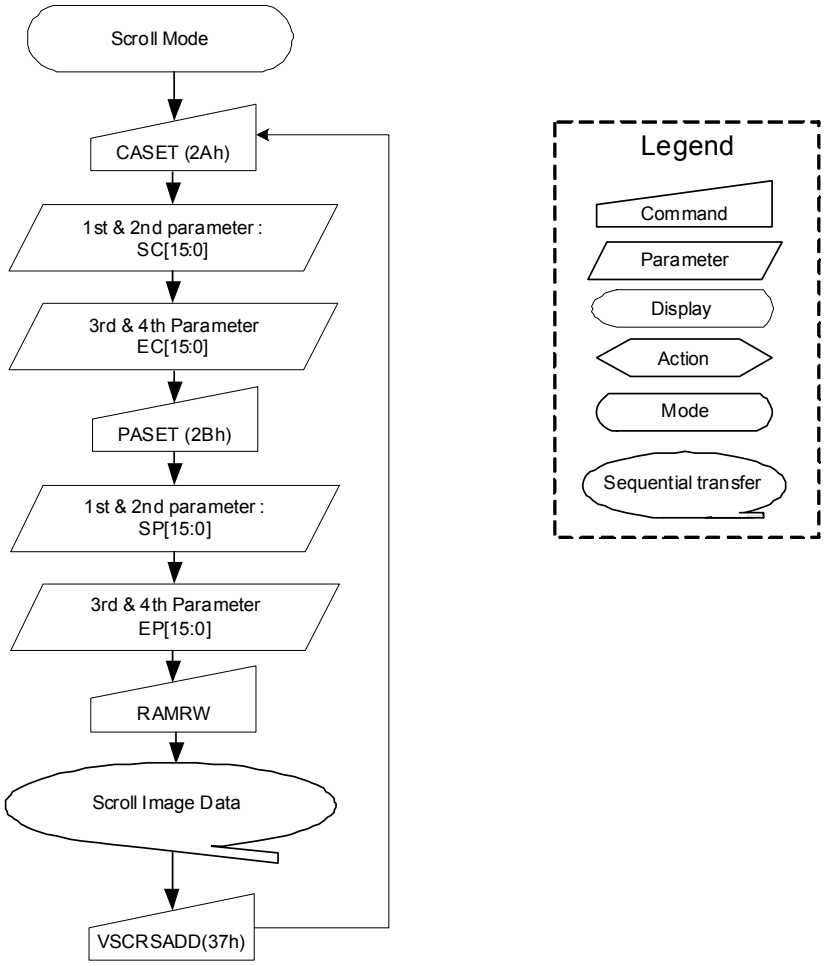
Flow Chart

1. To enter Vertical Scroll Mode :

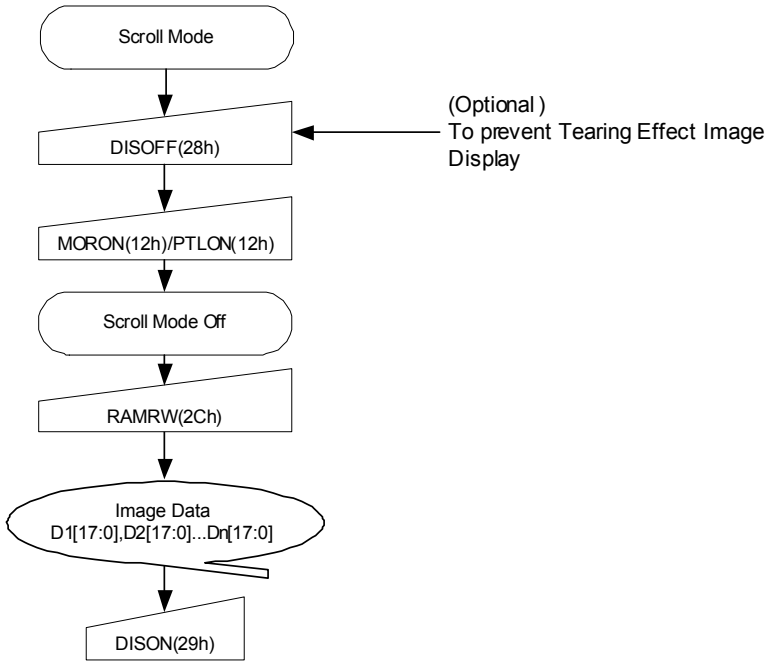


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll :



3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

8.2.27. Tearing Effect Line OFF (34h)

34h	TEOFF (Tearing Effect Line OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Parameter	No Parameter												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. X = Don't care.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

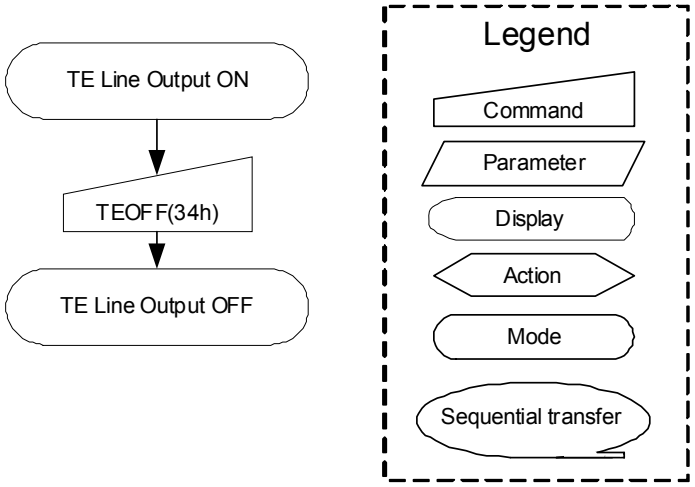
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



8.2.28. Tearing Effect Line ON (35h)

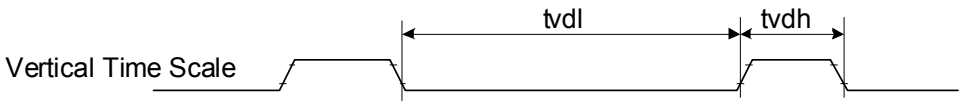
35h	TEON (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	M	00

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:

The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = Don't care.

Restriction

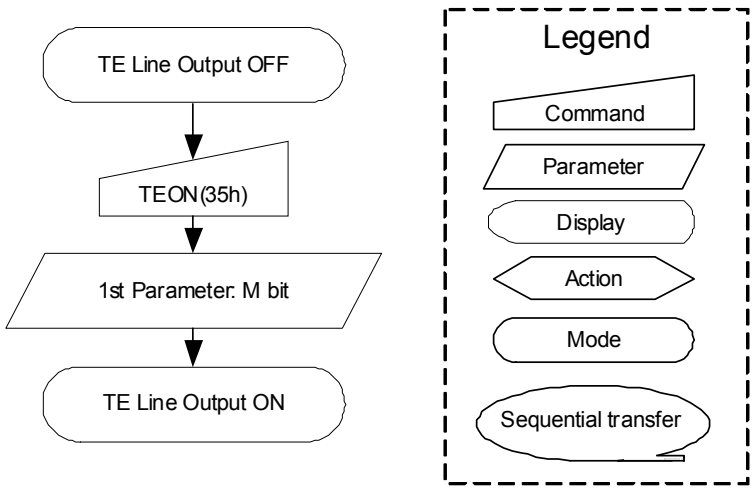
This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart	

8.2.29. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00

Description

This command defines read/write scanning direction of frame memory.

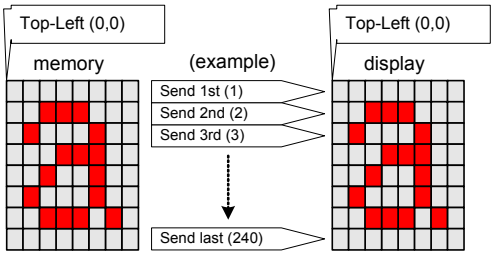
This command makes no change on the other driver status.

Bit	Name	Description
MY	Row Address Order	These 3 bits control MPU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

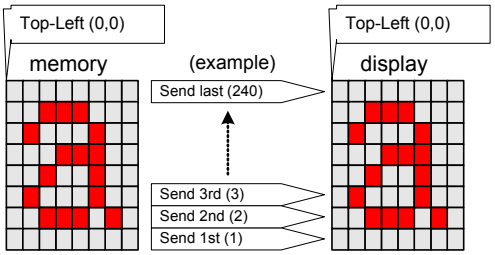
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

X = Don't care.

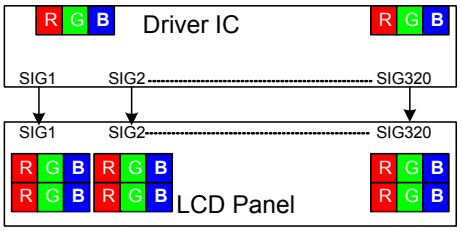
ML(Vertical refresh order bit)="0"



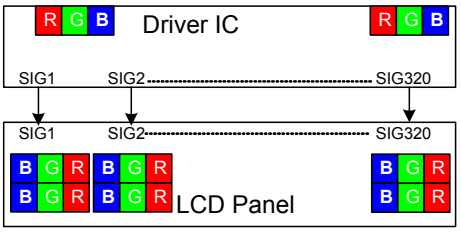
ML(Vertical refresh order bit)="1"

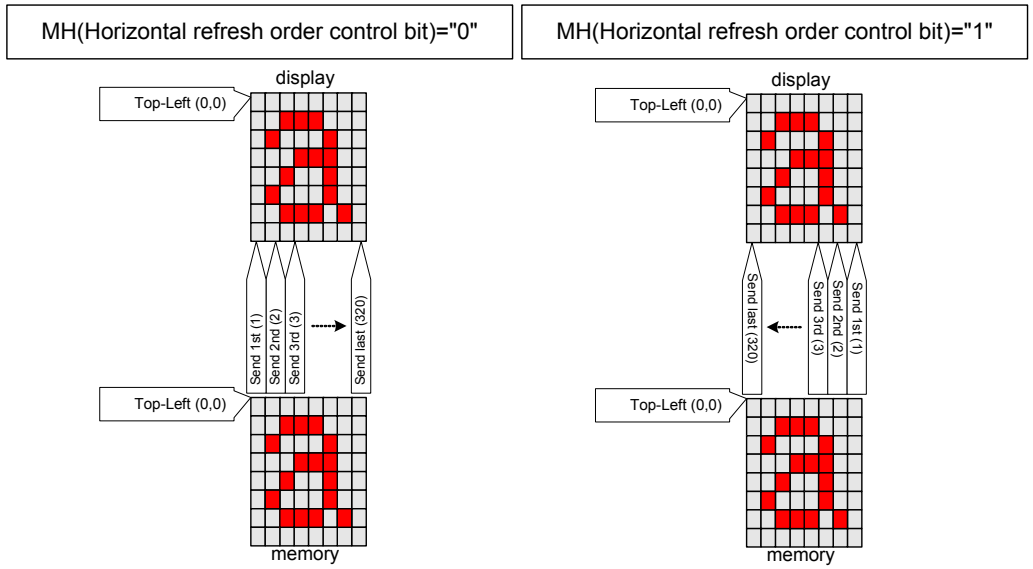


BGR(RGB-BGR Order control bit)="0"



BGR(RGB-BGR Order control bit)="1"





Note: Top-Left (0,0) means a physical memory location.

Restriction

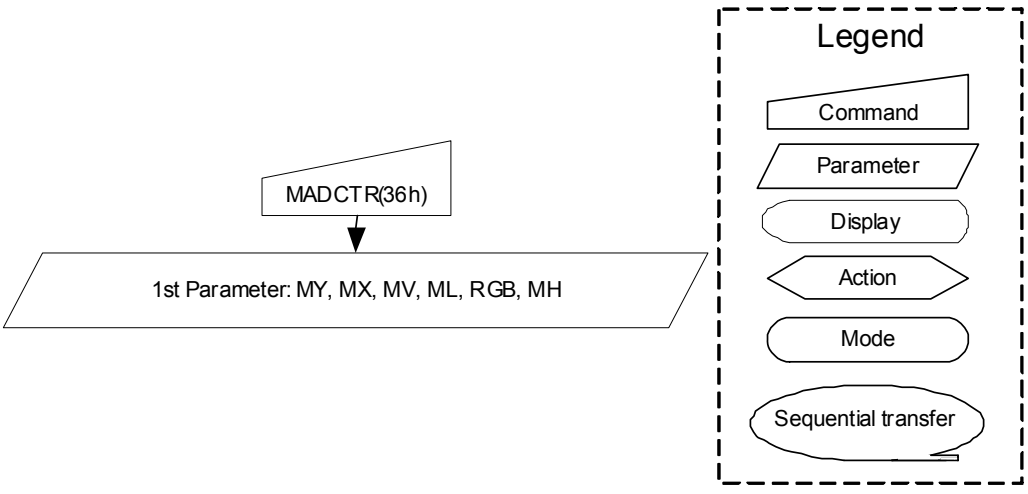
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No change
HW Reset	8'h00h

Flow Chart



8.2.30. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	↑	1	XX	VSP [15:8]								00
2nd Parameter	1	↑	1	XX	VSP [7:0]								00

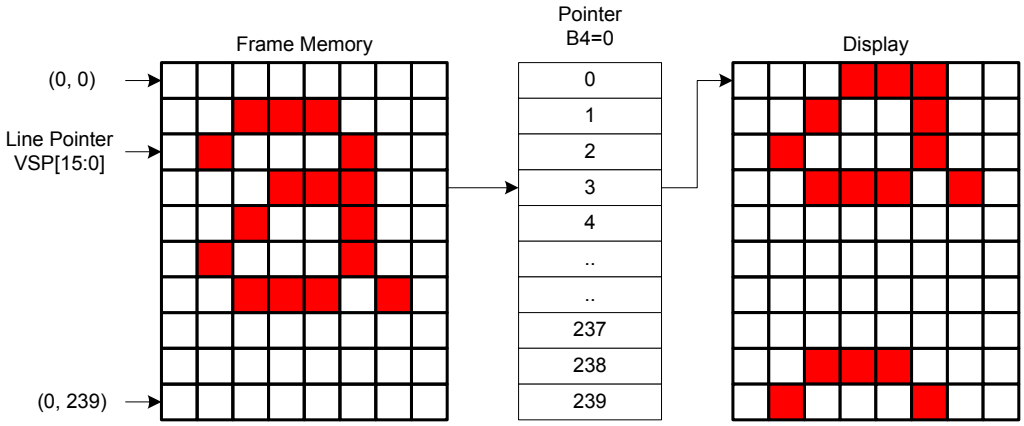
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

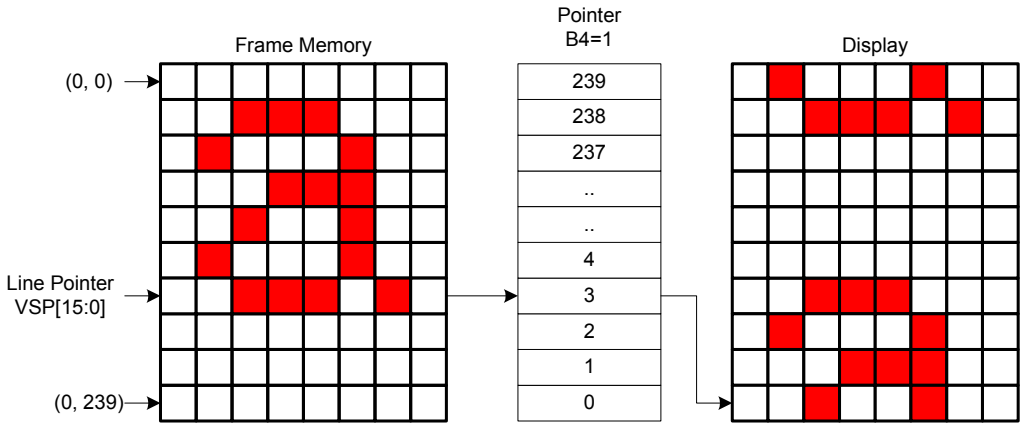
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP='3'.



When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

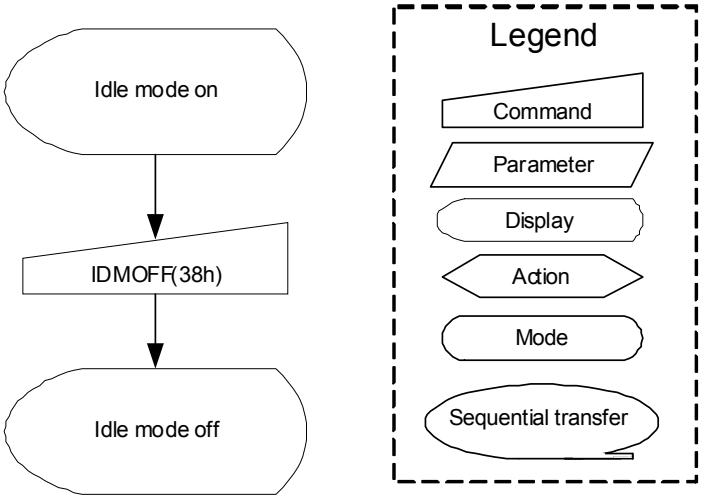
(2) This command is ignored when the ILI9342 enters Partial mode.

X = Don't care

Restriction

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

8.2.31. Idle Mode OFF (38h)

<table>
<tr><th>38h</th><th colspan="13">IDMOFF (Idle Mode OFF)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

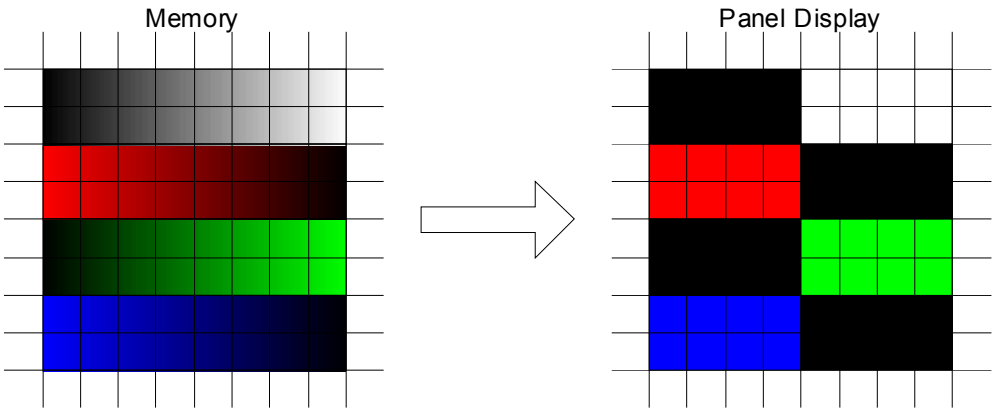
8.2.32. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter												

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory Contents vs. Display Color			
	$R_5\ R_4\ R_3\ R_2\ R_1\ R_0$	$G_5\ G_4\ G_3\ G_2\ G_1\ G_0$	$B_5\ B_4\ B_3\ B_2\ B_1\ B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = Don't care.

Restriction

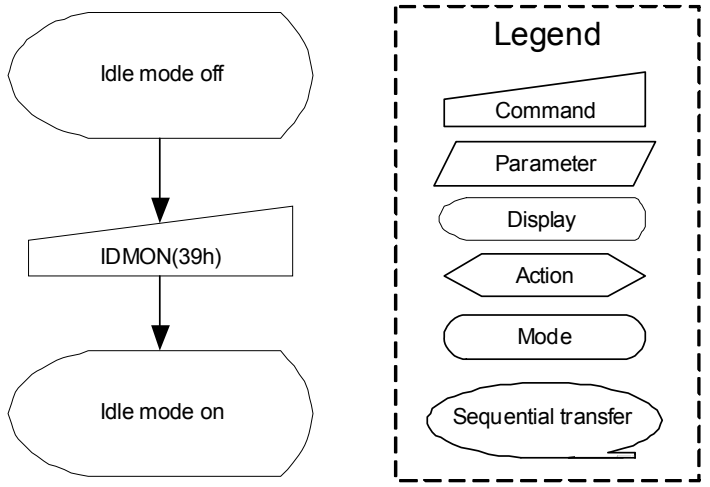
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart	

8.2.33. COLMOD: Pixel Format Set (3Ah)

3Ah	PIXSET (Pixel Format Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	1	1	0	3Ah
Parameter	1	1	↑	XX	0	DPI [2:0]			0	DBI [2:0]			66

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MPU interface. If a particular interface, either RGB interface or MPU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	12 bits / pixel
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

DBI [2:0]			MPU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	12 bits / pixel
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

X = Don't care

Restriction

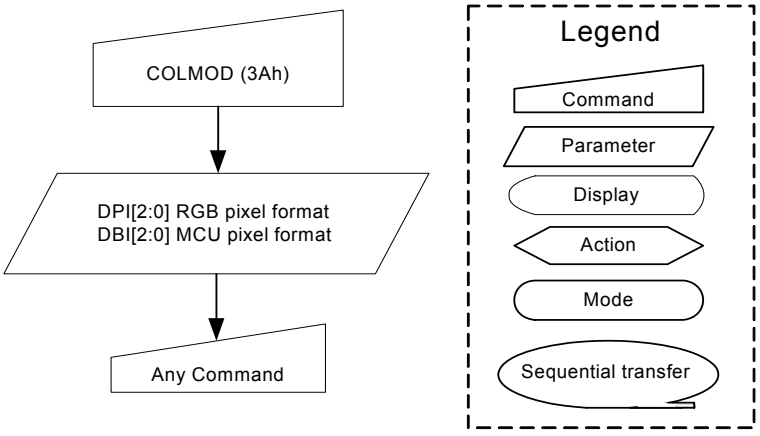
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b110	3'b110
SW Reset	No Change	No Change
HW Reset	3'b110	3'b110

Flow Chart



8.2.34. Write Memory Continue (3Ch)

3Ch	Write Memory Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	D1[17:0]									00000 3FFFF
Xth Parameter	1	1	↑	DX[17:0]									00000 3FFFF
Nth Parameter	1	1	↑	DN[17:0]									00000 3FFFF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or write memory start command. **If MADCTL B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write memory start or write memory continues. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If MADCTL B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write memory start or write memory continues. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.												
Restriction	A write memory start should follow a set column address, set page address or set address mode to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.												

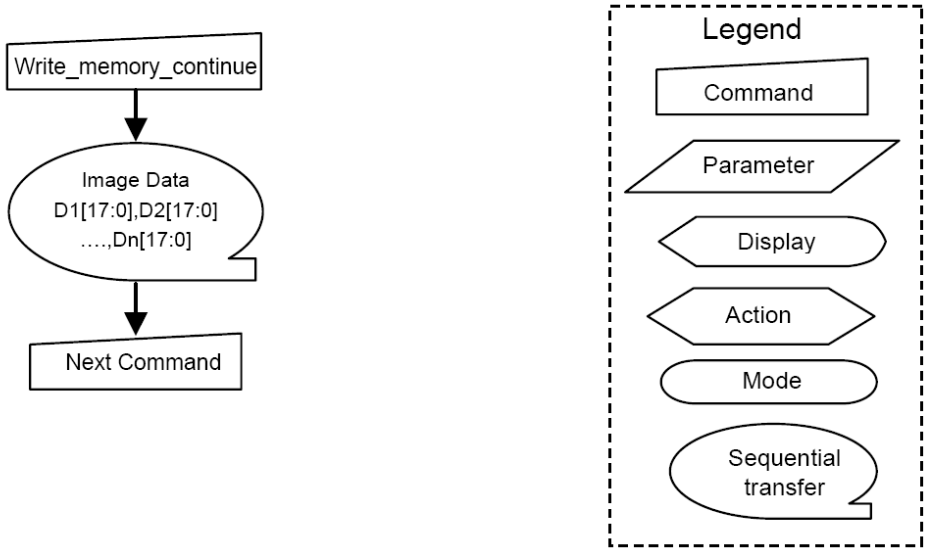
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	No

Default

Status	Default Value
Power On Sequence	Random value
SW Reset	No change
HW Reset	No change

Flow Chart



8.2.35. Read Memory Continue (3Eh)

3Eh	Read Memory Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D1[17:0]									00000 3FFFF
xst Parameter	1	↑	1	DX[17:0]									00000 3FFFF
Nst Parameter	1	↑	1	DN[17:0]									00000 3FFFF

Description

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read memory continue (3Eh) or read memory start (2Eh) command.

If MADCTL B5 = 0:

Pixels are read continuing from the pixel location after the read range of the previous read memory start or read memory continues. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.

If MADCTL B5 = 1:

Pixels are read continuing from the pixel location after the read range of the previous read memory start or read memory continues. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.

This command makes no change to the other driver status.

Restriction

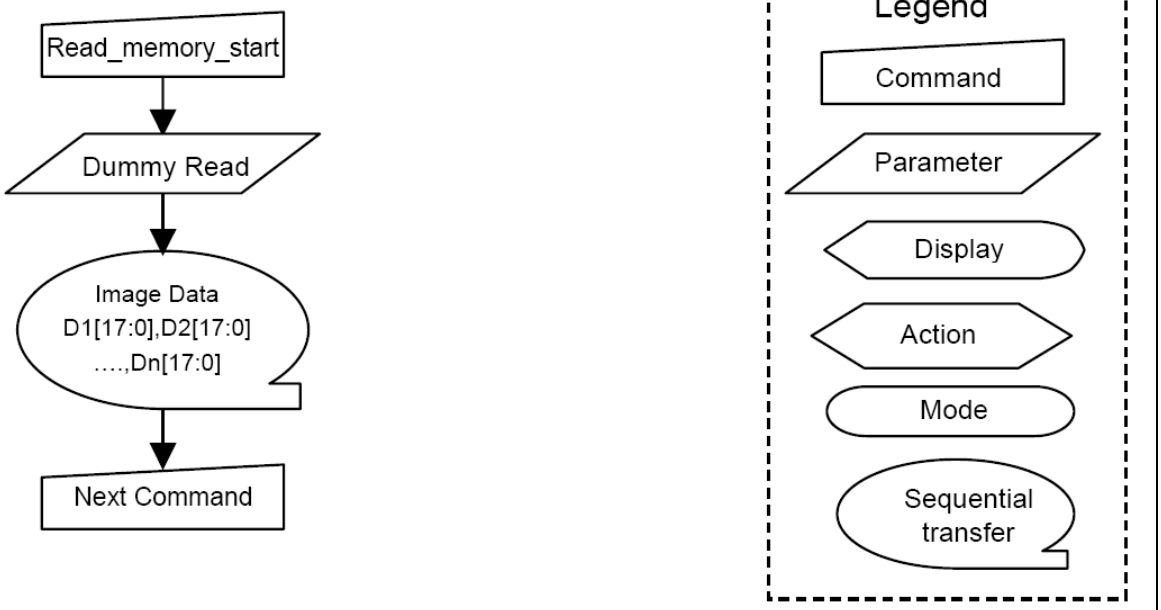
A read memory start should follow a set column address, set page address or set address mode to define the read location. Otherwise, data read with read memory continue is undefined.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random data
SW Reset	No change
HW Reset	No change

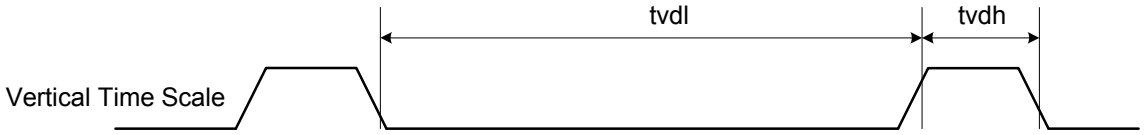
Flow Chart	

8.2.36. Set Tear Scan line (44h)

44h	Set Tear Scan line												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	STS[8]	00
2nd Parameter	1	1	↑	XX	STS[7:0]								00

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



Note that set tear scan line with N=0 is equivalent to set tear on with M=0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

-

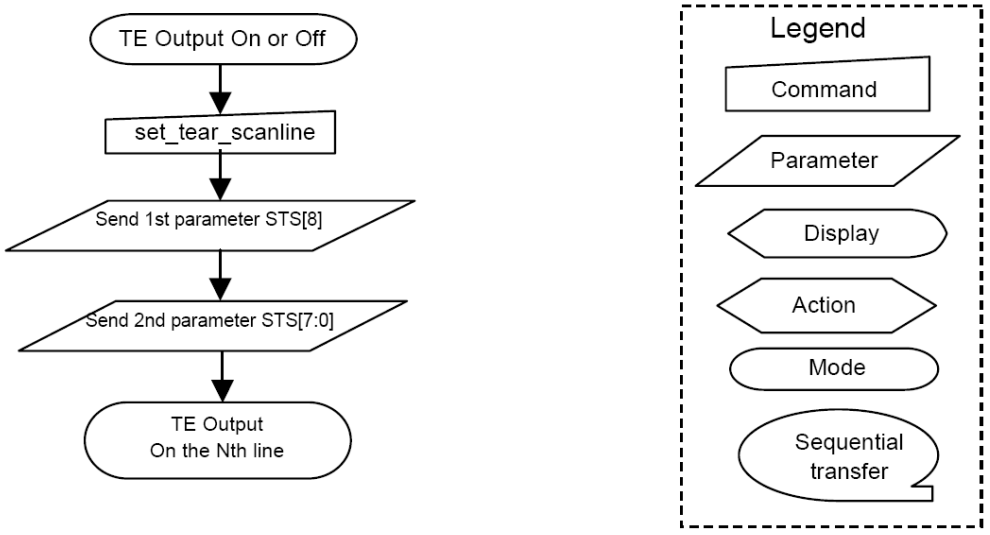
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS [8:0]=0000h
SW Reset	STS [8:0]=0000h
HW Reset	STS [8:0]=0000h

Flow Chart



8.2.37. Get Scan line (45h)

45h	Get Scan line												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	0	0	0	0	0	GTS[9:8]		00
3rd Parameter	1	↑	1	XX	GTS[7:0]								00
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get scan line is undefined.												
Restriction	None												

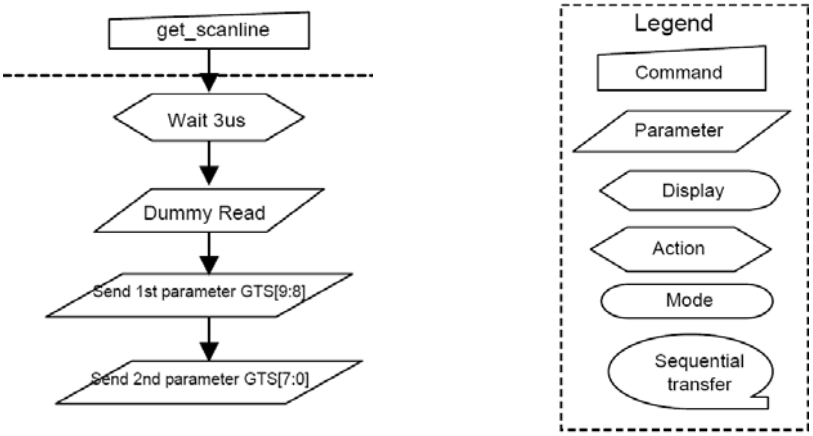
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GTS [9:0]
Power On Sequence	GTS [9:0]=0000h
SW Reset	GTS [9:0]=0000h
HW Reset	GTS [9:0]=0000h

Flow Chart



8.2.38. Read ID1 (DAh)

DAh	RDID1 (Read ID1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID1 [7:0]								XX
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID. X = Don't care												
Restriction													

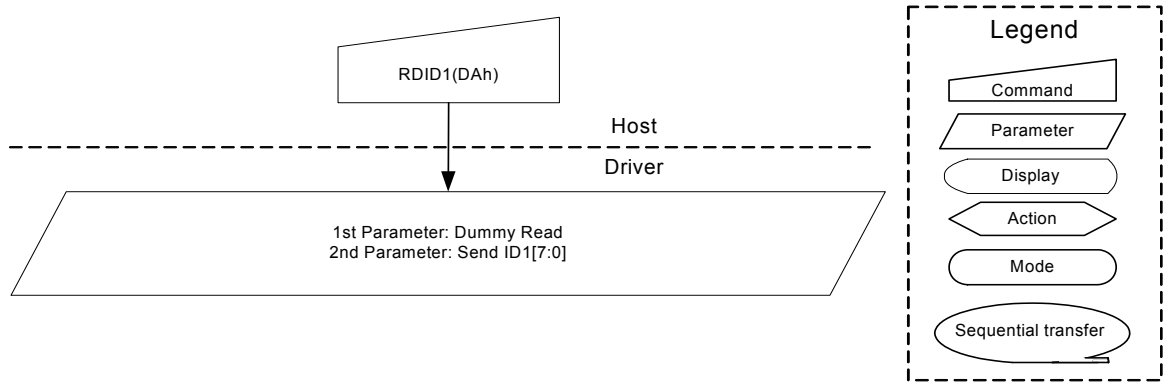
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



8.2.39. Read ID2 (DBh)

DBh	RDID2 (Read ID2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	1	ID2 [6:0]							XX
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID2 can be programmed by MTP function. X = Don't care												
Restriction													

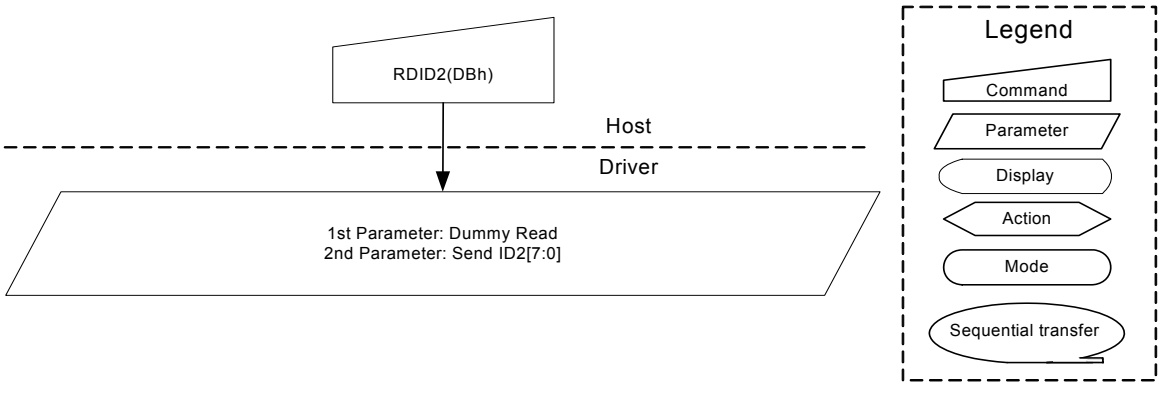
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h80h	MTP value
SW Reset	8'h80h	MTP value
HW Reset	8'h80h	MTP value

Flow Chart



8.2.40. Read ID3 (DCh)

DCh	RDID3 (Read ID3)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								XX
Description	This read byte identifies the LCD module/driver and It is specified by User. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver ID. The ID3 can be programmed by MTP function. X = Don't care												
Restriction													

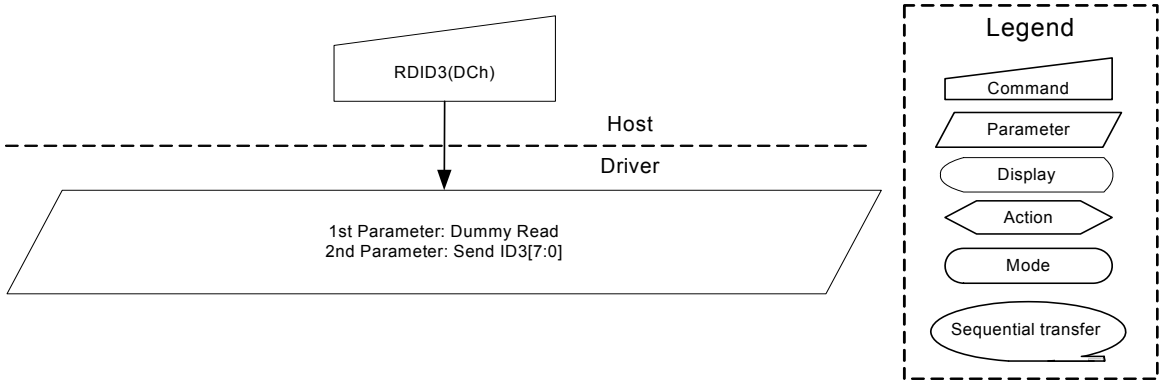
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



8.3. Description of Extended Command set

8.3.1. RGB Interface Signal Control (B0h)

<table>
<tr><th>B0h</th><th colspan="13">IFMODE (Interface Mode Control)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>BYPASS</td><td colspan="2">RCM[1:0]</td><td>0</td><td>VSPL</td><td>HSPL</td><td>DPL</td><td>EPL</td><td>40</td></tr>
<tr><td>Description</td><td colspan="13">Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

EPL: DE polarity (“0”= High enable for RGB interface, “1”= Low enable for RGB interface)

DPL: DOTCLK polarity set (“0”= data fetched at the rising time, “1”= data fetched at the falling time)

HSPL: HSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)

VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)

RCM [1:0]: RGB interface selection (refer to the RGB interface section).

<table>
<tr><th colspan="2">RCM [1:0]</th><th>RGB transfer mode</th></tr>
<tr><td>1</td><td>0</td><td rowspan="2">DE Mode</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td rowspan="2">SYNC Mode</td></tr>
<tr><td>1</td><td>1</td></tr>
</table>

BYPASS: Select display data path whether Memory or Direct to Shift register when RGB Interface is used.

<table>
<tr><th>BYPASS</th><th>Display Data Path</th></tr>
<tr><td>0</td><td>Direct to Shift Register (default)</td></tr>
<tr><td>1</td><td>Memory</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="6">Default Value</th></tr>
<tr><th>BYPASS</th><th>RCM [1:0]</th><th>VSPL</th><th>HSPL</th><th>DPL</th><th>EPL</th></tr>
<tr><td>Power ON Sequence</td><td>1’b0</td><td>2’b10</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>1’b0</td><td>2’b10</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>1’b0</td><td>2’b10</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
</table>
</td></tr>
</table>

8.3.2. Display Waveform Cycle 1 (In Normal Mode/Full Colors) (B1h)

B1h	CYCSET1 (Set Display Waveform Cycle In Normal Mode / Full colors)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVA [1:0]		00
2nd Parameter	1	1	↑	XX	0	0	0	RTNA [4:0]					1B

Description

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Normal mode at MPU interface.

RTNA [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNA [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNA [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVA [1:0]	RTNA [4:0]
Power ON Sequence	2'b00	5'h1Bh
SW Reset	2'b00	5'h1Bh
HW Reset	2'b00	5'h1Bh

8.3.3. Display Waveform Cycle 2 (In Idle Mode/8 colors) (B2h)

B2h	CYCSET2 (Set Display Waveform Cycle In Idle Mode / 8 colors)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVB [1:0]		00
2ndParameter	1	1	↑	XX	0	0	0	RTNB [4:0]					1B

Description

DIVB [1:0]: division ratio for internal clocks when Idle mode.

DIVB [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNB [4:0]: RTNB[4:0] is used to set 1H (line) period of Idle mode at MPU interface.

RTNB [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNB [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNB [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVB [1:0]	RTNB [4:0]
Power ON Sequence	2'b00	5'h1Bh
SW Reset	2'b00	5'h1Bh
HW Reset	2'b00	5'h1Bh

8.3.4. Display Waveform Cycle (In Partial Mode/Full Colors) (B3h)

B3h	CYCSET3 (Set Display Waveform Cycle In Partial Mode / Full colors)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC [1:0]		00
2ndParameter	1	1	↑	XX	0	0	0	RTNC [4:0]					1B

Description

DIVC [1:0]: division ratio for internal clocks when Partial mode.

DIVC [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of Partial mode at MPU interface.

RTNC [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNC [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNC [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVC [1:0]	RTNC [4:0]
Power ON Sequence	2'b00	5'h1Bh
SW Reset	2'b00	5'h1Bh
HW Reset	2'b00	5'h1Bh

8.3.5. Display Inversion Control (B4h)

B4h	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XX	0	0	0	0	0	NLA	NLB	NLC	02
2ndParameter	1	1	↑	XX	0	0	NW [5:0]						00

Description

Display inversion mode set

NLA: Inversion setting in full colors normal mode (Normal mode on)

NLB: Inversion setting in Idle mode (Idle mode on)

NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLA / NLB / NLC	Inversion
0	Line inversion
1	Frame inversion

NW [5:0]: N-line inversion setting in NLA=0, NLB=0 and NLC=0.

NW [5:0]						N-line Inversion
0	0	0	0	0	0	1 lines
0	0	0	0	0	1	2 lines
0	0	0	0	1	0	3 lines
0	0	0	0	1	1	4 lines
0	0	0	1	0	0	5 lines
0	0	0	1	0	1	6 lines
0	0	0	1	1	0	7 lines
0	0	0	1	1	1	8 lines
0	0	1	0	0	0	9 lines
0	0	1	0	0	1	10 lines
0	0	1	0	1	0	11 lines
0	0	1	0	1	1	12 lines
0	0	1	1	0	0	13 lines
0	0	1	1	0	1	14 lines
0	0	1	1	1	0	15 lines
0	0	1	1	1	1	16 lines
0	1	0	0	0	0	17 lines
0	1	0	0	0	1	18 lines
0	1	0	0	1	0	19 lines
0	1	0	0	1	1	20 lines
0	1	0	1	0	0	21 lines
0	1	0	1	0	1	22 lines
0	1	0	1	1	0	23 lines
0	1	0	1	1	1	24 lines
0	1	1	0	0	0	25 lines
0	1	1	0	0	1	26 lines
0	1	1	0	1	0	27 lines
0	1	1	0	1	1	28 lines
0	1	1	1	0	0	29 lines
0	1	1	1	0	1	30 lines
0	1	1	1	1	0	31 lines
0	1	1	1	1	1	32 lines

NW [5:0]						N-line Inversion
1	0	0	0	0	0	33 lines
1	0	0	0	0	1	34 lines
1	0	0	0	1	0	35 lines
1	0	0	0	1	1	36 lines
1	0	0	1	0	0	37 lines
1	0	0	1	0	1	38 lines
1	0	0	1	1	0	39 lines
1	0	0	1	1	1	40 lines
1	0	1	0	0	0	41 lines
1	0	1	0	0	1	42 lines
1	0	1	0	1	0	43 lines
1	0	1	0	1	1	44 lines
1	0	1	1	0	0	45 lines
1	0	1	1	0	1	46 lines
1	0	1	1	1	0	47 lines
1	0	1	1	1	1	48 lines
1	1	0	0	0	0	49 lines
1	1	0	0	0	1	50 lines
1	1	0	0	1	0	51 lines
1	1	0	0	1	1	52 lines
1	1	0	1	0	0	53 lines
1	1	0	1	0	1	54 lines
1	1	0	1	1	0	55 lines
1	1	0	1	1	1	56 lines
1	1	1	0	0	0	57 lines
1	1	1	0	0	1	58 lines
1	1	1	0	1	0	59 lines
1	1	1	0	1	1	60 lines
1	1	1	1	0	0	61 lines
1	1	1	1	0	1	62 lines
1	1	1	1	1	0	63 lines
1	1	1	1	1	1	64 lines

Restriction	SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value			
	NLA	NLB	NLC	NW [5:0]
Power ON Sequence	1'b0	1'b1	1'b0	6'h00h
SW Reset	1'b0	1'b1	1'b0	6'h00h
H/W Reset	1'b0	1'b1	1'b0	6'h00h

8.3.6. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	0	VFP [6:0]							02
2nd Parameter	1	1	↑	XX	0	VBP [6:0]							02
3rd Parameter	1	1	↑	XX	0	0	0	HFP [4:0]					0A
4th Parameter	1	1	↑	XX	0	0	0	HBP [4:0]					14

Description

VFP [6:0] / VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HFP [4:0] / HBP [4:0]: The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.

HFP [4:0] HBP [4:0]	Number of DOTCLK of the front/back porch
00000	Setting prohibited
00001	Setting prohibited
00010	2
00011	3
00100	4
00101	5
00110	6
00111	7
01000	8
01001	9
01010	10
01011	11
01100	12
01101	13
01110	14
01111	15

HFP [4:0] HBP [4:0]	Number of DOTCLK of front/back porch
10000	16
10001	17
10010	18
10011	19
10100	20
10101	21
10110	22
10111	23
11000	24
11001	25
11010	26
11011	27
11100	28
11101	29
11110	30
11111	31

<table>
<tr><td>Restriction</td><td>SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HFP [4:0]</th><th>HBP [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
<tr><td>SW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
<tr><td>HW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
</table>
</td></tr>
</table>

8.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	0	0	0	0	PTG [1:0]		PT [1:0]		0A
2nd Parameter	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				02
3rd Parameter	1	1	↑	XX	0	0	NL [5:0]						27
4th Parameter	1	1	↑	XX	X	X	PCDIV[5:0]						04

Description

PTG [1:0]: Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Set with the PT [2:0] bits	VCOMH/VCOML
0	1	Setting prohibited	---	---
1	0	Interval scan	Set with the PT [2:0] bits	
1	1	Setting prohibited	---	---

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT [1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive polarity	Negative polarity	Positive polarity	Negative polarity
0	0	V63	V0	VCOML	VCOMH
0	1	V0	V63	VCOML	VCOMH
1	0	AGND	AGND	AGND	AGND
1	1	Hi-Z	Hi-Z	AGND	AGND

SS: This bit controls MPU to memory write/read direction by column address order.

REV: Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

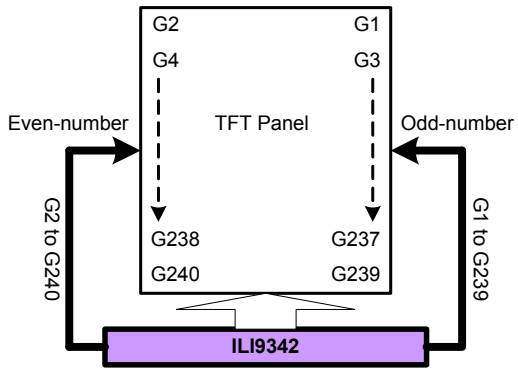
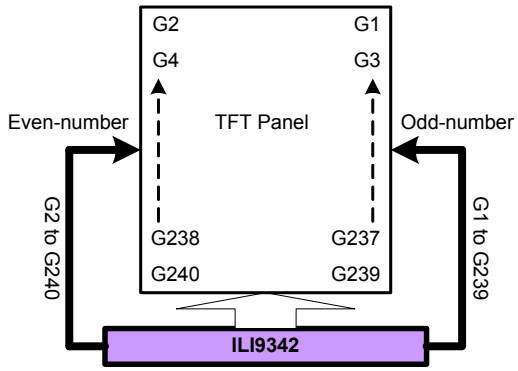
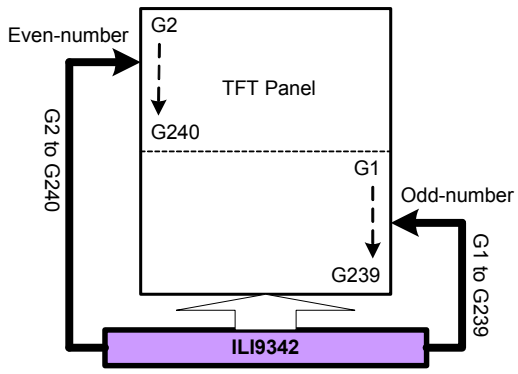
Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

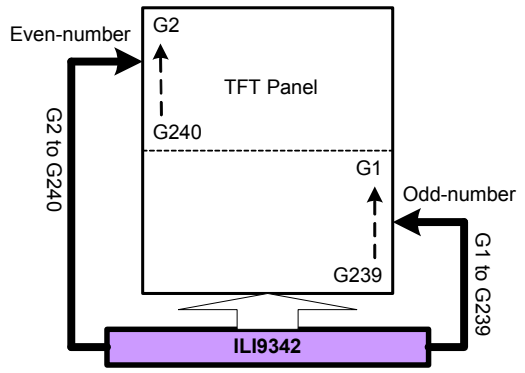
ISC [3:0]	Scan Cycle	f_{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms
1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1 → G240
1	G240 → G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G237→G238→G239→G240
0	1		G240→G239->G238→G237→…… …. →G4→G3→G2→G1
1	0		G1→G3→…….....→G237→G239→ G2→G4→……→G238→G240

1	1		G240, G238, G236, …, G10, G8, G6, G4, G2 G239, G237, G235, …, G9, G78, G5, G3, G1 G240→G238→…….→G4→G2→ G239→G237→……→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

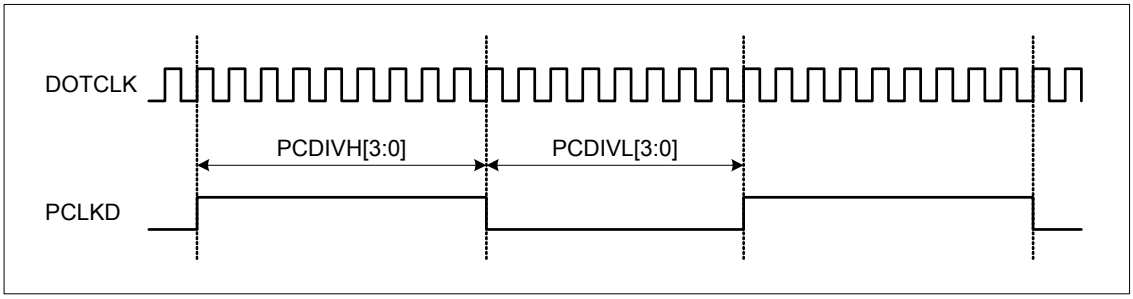
NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

NL [5:0]						LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
Others						Setting inhibited

PCDIVH [3:0]: Number of DOTCLK during internal clock CLKD's high period. In units of 1 clock.

PCDIVL [3:0]: Number of DOTCLK during internal clock CLKD's low period. In units of 1 clock.

PCDIVH and PCDIVL, specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 678KHz is the smallest. Set PCDIVL = PCDIVH or PCDIVL - 1.



$$External\ \ fosc = \frac{\text{DOTCLK}}{2 \times (\frac{\text{PCDIVH}}{\text{PCDIVL}} + 1)}$$

Restriction	SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value							
	PTG [1:0]	PT [1:0]	REV	GS	SS	SM	ISC [3:0]	NL [5:0]
Power ON Sequence	2'b10	2'b10	1'b0	1'b0	1'b0	1'b0	4'b0010	6'h27h
SW Reset	2'b10	2'b10	1'b0	1'b0	1'b0	1'b0	4'b0010	6'h27h
HW Reset	2'b10	2'b10	1'b0	1'b0	1'b0	1'b0	4'b0010	6'h27h

8.3.8. Entry Mode Set (B7h)

B7h	ETMOD (Entry Mode Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
Parameter	1	1	↑	XX	0	0	0	0	DSTB	GON	DTE	GAS	07

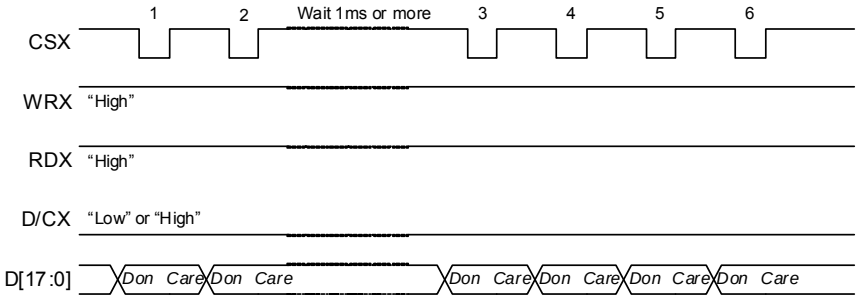
Description

DSTB: The ILI9342 driver enters the Deep Standby Mode when DSTB is set to high ("1"). In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited.

Note: ILI9342 provides two ways to exit the Deep Standby Mode:

(1) Exit Deep Standby Mode by pull down CSX to low ("0") 6 times.

(2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state.



GAS: Low voltage detection control.

GAS	Low voltage detection
0	Enable
1	Disable

GON/DTE: Set the output level of gate driver G1 ~ G240 as follows

GON	DTE	G1~G240 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value			
	DSTB	GON	DTE	GAS
Power ON Sequence	1'b0	1'b1	1'b1	1'b1
SW Reset	1'b0	1'b1	1'b1	1'b1
HW Reset	1'b0	1'b1	1'b1	1'b1

8.3.9. Oscillator Control (B8h)

B1h	OSCCTR (Oscillator Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
1st Parameter	1	1	↑	XX	0	0	0	0	FOSC[3:0]				00

Description

FOSC[3:0] : Set the oscillation frequency of internal oscillator

FOSC [3:0]				Frame Rate (Hz)
0	0	0	0	43
0	0	0	1	47
0	0	1	0	51
0	0	1	1	55
0	1	0	0	61
0	1	0	1	64
0	1	1	0	67
0	1	1	1	71
1	0	0	0	76
1	0	0	1	87
1	0	1	0	93
1	0	1	1	93
1	1	0	0	93
1	1	0	1	93
1	1	1	0	93
1	1	1	1	93

Formula to calculate frame frequency:

$$Frame\ Rate = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Normal mode at MPU interface.

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNA setting

Division ratio : DIVA setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
	FOSC [3:0]
Power ON Sequence	4'b0111
SW Reset	4'b0111
HW Reset	4'b0111

8.3.10. Set EXTC (B9h)

B9h	SETEXTC (Set EXTC)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
1st Parameter	1	1	↑	XX	EXTC1[7:0]								00
2nd Parameter	1	1	↑	XX	EXTC2[7:0]								00
3rd Parameter	1	1	↑	XX	EXTC3[7:0]								00
Description	Turn on the external command if setting EXTC1[7:0] = 0xFF, EXTC2[7:0] = 0x93, and EXTC3[7:0] = 0x42												
Restriction													

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value		
	EXTC1[7:0]	EXTC2[7:0]	EXTC3[7:0]
Power ON Sequence	00h	00h	00h
SW Reset	00h	00h	00h
HW Reset	00h	00h	00h

8.3.11. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
1st Parameter	1	1	↑	XX	0	0	VRH [5:0]						26
2nd Parameter	1	1	↑	XX	0	0	0	0	VC [3:0]				00

Description

VRH [5:0]: Set the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VRH [5:0]						VREG1OUT
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	Setting prohibited
0	0	0	0	1	0	Setting prohibited
0	0	0	0	1	1	3.00 V
0	0	0	1	0	0	3.05 V
0	0	0	1	0	1	3.10 V
0	0	0	1	1	0	3.15 V
0	0	0	1	1	1	3.20 V
0	0	1	0	0	0	3.25 V
0	0	1	0	0	1	3.30 V
0	0	1	0	1	0	3.35 V
0	0	1	0	1	1	3.40 V
0	0	1	1	0	0	3.45 V
0	0	1	1	0	1	3.50 V
0	0	1	1	1	0	3.55 V
0	0	1	1	1	1	3.60 V
0	1	0	0	0	0	3.65 V
0	1	0	0	0	1	3.70 V
0	1	0	0	1	0	3.75 V
0	1	0	0	1	1	3.80 V
0	1	0	1	0	0	3.85 V
0	1	0	1	0	1	3.90 V
0	1	0	1	1	0	3.95 V
0	1	0	1	1	1	4.00 V
0	1	1	0	0	0	4.05 V
0	1	1	0	0	1	4.10 V
0	1	1	0	1	0	4.15 V
0	1	1	0	1	1	4.20 V
0	1	1	1	0	0	4.25 V
0	1	1	1	0	1	4.30 V
0	1	1	1	1	0	4.35 V
0	1	1	1	1	1	4.40 V

VRH [5:0]						VREG1OUT
1	0	0	0	0	0	4.45 V
1	0	0	0	0	1	4.50 V
1	0	0	0	1	0	4.55 V
1	0	0	0	1	1	4.60 V
1	0	0	1	0	0	4.65 V
1	0	0	1	0	1	4.70 V
1	0	0	1	1	0	4.75 V
1	0	0	1	1	1	4.80 V
1	0	1	0	0	0	4.85 V
1	0	1	0	0	1	4.90 V
1	0	1	0	1	0	4.95 V
1	0	1	0	1	1	5.00 V
1	0	1	1	0	0	5.05 V
1	0	1	1	0	1	5.10 V
1	0	1	1	1	0	5.15 V
1	0	1	1	1	1	5.20 V
1	1	0	0	0	0	5.25 V
1	1	0	0	0	1	5.30 V
1	1	0	0	1	0	5.35 V
1	1	0	0	1	1	5.40 V
1	1	0	1	0	0	5.45 V
1	1	0	1	0	1	5.50 V
1	1	0	1	1	0	5.55 V
1	1	0	1	1	1	5.60 V
1	1	1	0	0	0	5.65 V
1	1	1	0	0	1	5.70 V
1	1	1	0	1	0	5.75 V
1	1	1	0	1	1	5.80 V
1	1	1	1	0	0	5.85 V
1	1	1	1	0	1	5.90 V
1	1	1	1	1	0	5.95 V
1	1	1	1	1	1	6.00 V

Note1: Make sure that VC and VRH setting restriction: VREG1OUT ≦ (DDVDH - 0.5) V.

VC [3:0]: Sets VCI1 internal reference regulator voltage.

VC [3:0]				VCI1 Voltage
0	0	0	0	2.30V
0	0	0	1	2.35V
0	0	1	0	2.40V
0	0	1	1	2.45V
0	1	0	0	2.50V
0	1	0	1	2.55V
0	1	1	0	2.60V
0	1	1	1	2.65V
1	0	0	0	2.70V
1	0	0	1	2.75V
1	0	1	0	2.80V
1	0	1	1	2.85V
1	1	0	0	2.90V
1	1	0	1	2.95V
1	1	1	0	3.00V
1	1	1	1	External VCI

Note: Do not set any higher VCI1 level than VCI - 0.2V.

<table>
<tr><td>Restriction</td><td>SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>VC [3:0]</th><th>VRH [5:0]</th></tr>
<tr><td>Power ON Sequence</td><td>4’b0000</td><td>6’h26h</td></tr>
<tr><td>SW Reset</td><td>4’b0000</td><td>6’h26h</td></tr>
<tr><td>HW Reset</td><td>4’b0000</td><td>6’h26h</td></tr>
</table>
</td></tr>
</table>

8.3.12. Power Control 2 (C1h)

C1h	PWCTRL 2 (Power Control 2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
Parameter	1	1	↑	XX	0	SAP [2:0]			BT [3:0]				10

Description

BT [3:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT [3:0]				DDVDH	VGH	VGL
0	0	0	0	VCI1 x 2	VCI1 x 6	-VCI1 x 5
0	0	0	1			-VCI1 x 4
0	0	1	0			-VCI1 x 3
0	0	1	1		VCI1 x 5	-VCI1 x 5
0	1	0	0			-VCI1 x 4
0	1	0	1			-VCI1 x 3
0	1	1	0		VCI1 x 4	-VCI1 x 4
0	1	1	1			-VCI1 x 3
1	0	0	0	VCI1 x 3	VCI1 x 9	-VCI1 x 7
1	0	0	1			-VCI1 x 6
1	0	1	0			-VCI1 x 4
1	0	1	1		VCI1 x 7	-VCI1 x 7
1	1	0	0			-VCI1 x 6
1	1	0	1			-VCI1 x 4
1	1	1	0		VCI1 x 6	-VCI1 x 6
1	1	1	1			-VCI1 x 4

Note1: Make sure that DDVDH setting restriction: DDVDH ≦ 6.0 V.

2: Make sure that VGH and VGL setting restriction: VGH -VGL ≦ 32 V.

SAP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set SAP[2:0] = "000" to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

SAP[2:0]	Gamma driver amplifiers	Source driver amplifiers
000	Halt	Halt
001	1.00	1.00
010	1.00	0.75
011	1.00	0.50
100	0.75	1.00
101	0.75	0.75
110	0.75	0.50
111	0.50	0.50

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	BT [3:0]	SAP [2:0]
Power ON Sequence	4'b0000	3'b001
SW Reset	4'b0000	3'b001
HW Reset	4'b0000	3'b001

8.3.13. Power Control 3 (For Normal Mode) (C2h)

C2h	PWCTRL 3 (Power Control 3)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	0	C2h
Parameter	1	1	↑	XX	x	DCA1 [2:0]			x	DCA0 [2:0]			C2

Description

DCA0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCA1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCA0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	1/32 x H Line Frequency
0	0	1	1/16 x H Line Frequency
0	1	0	1/8 x H Line Frequency
0	1	1	1/4 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	1 x H Line Frequency
1	1	0	1 x H Line Frequency
1	1	1	1 x H Line Frequency

DCA1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	1/32 x H Line Frequency
0	0	1	1/16 x H Line Frequency
0	1	0	1/8 x H Line Frequency
0	1	1	1/4 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	1 x H Line Frequency
1	1	0	1 x H Line Frequency
1	1	1	1 x H Line Frequency

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCA0 [2:0]	DCA1 [2:0]
Power ON Sequence	3'b010	3'b001
SW Reset	3'b010	3'b001
HW Reset	3'b010	3'b001

8.3.14. Power Control 4 (For Idle Mode) (C3h)

C3h	PWCTRL 4 (Power Control 4)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
Parameter	1	1	↑	XX	X	DCB1 [2:0]			X	DCB0 [2:0]			C2

Description

DCB0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	1/32 x H Line Frequency
0	0	1	1/16 x H Line Frequency
0	1	0	1/8 x H Line Frequency
0	1	1	1/4 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	1 x H Line Frequency
1	1	0	1 x H Line Frequency
1	1	1	1 x H Line Frequency

DCB1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	1/32 x H Line Frequency
0	0	1	1/16 x H Line Frequency
0	1	0	1/8 x H Line Frequency
0	1	1	1/4 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	1 x H Line Frequency
1	1	0	1 x H Line Frequency
1	1	1	1 x H Line Frequency

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCB0 [2:0]	DCB1 [2:0]
Power ON Sequence	3'b010	3'b001
SW Reset	3'b010	3'b001
H/W Reset	3'b010	3'b001

8.3.15. Power Control 5 (For Partial Mode) (C4h)

C4h	PWCTRL 5 (Power Control 5)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
Parameter	1	1	↑	XX	X	DCC1 [2:0]			X	DCC0 [2:0]			C2

Description

DCC0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	1/32 x H Line Frequency
0	0	1	1/16 x H Line Frequency
0	1	0	1/8 x H Line Frequency
0	1	1	1/4 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	1 x H Line Frequency
1	1	0	1 x H Line Frequency
1	1	1	1 x H Line Frequency

DCC1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	1/32 x H Line Frequency
0	0	1	1/16 x H Line Frequency
0	1	0	1/8 x H Line Frequency
0	1	1	1/4 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	1 x H Line Frequency
1	1	0	1 x H Line Frequency
1	1	1	1 x H Line Frequency

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCC0 [2:0]	DCC1 [2:0]
Power ON Sequence	3'b010	3'b001
SW Reset	3'b010	3'b001
HW Reset	3'b010	3'b001

8.3.16. VCOM Control 1(C5h)

C5h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
1st Parameter	1	1	↑	XX	0	VMH [6:0]							31
2nd Parameter	1	1	↑	XX	0	VML [6:0]							3C

Description

VMH [6:0] : Set the VCOMH voltage.

VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)
0000000	2.700	0100000	3.500	1000000	4.300	1100000	5.100
0000001	2.725	0100001	3.525	1000001	4.325	1100001	5.125
0000010	2.750	0100010	3.550	1000010	4.350	1100010	5.150
0000011	2.775	0100011	3.575	1000011	4.375	1100011	5.175
0000100	2.800	0100100	3.600	1000100	4.400	1100100	5.200
0000101	2.825	0100101	3.625	1000101	4.425	1100101	5.225
0000110	2.850	0100110	3.650	1000110	4.450	1100110	5.250
0000111	2.875	0100111	3.675	1000111	4.475	1100111	5.275
0001000	2.900	0101000	3.700	1001000	4.500	1101000	5.300
0001001	2.925	0101001	3.725	1001001	4.525	1101001	5.325
0001010	2.950	0101010	3.750	1001010	4.550	1101010	5.350
0001011	2.975	0101011	3.775	1001011	4.575	1101011	5.375
0001100	3.000	0101100	3.800	1001100	4.600	1101100	5.400
0001101	3.025	0101101	3.825	1001101	4.625	1101101	5.425
0001110	3.050	0101110	3.850	1001110	4.650	1101110	5.450
0001111	3.075	0101111	3.875	1001111	4.675	1101111	5.475
0010000	3.100	0110000	3.900	1010000	4.700	1110000	5.500
0010001	3.125	0110001	3.925	1010001	4.725	1110001	5.525
0010010	3.150	0110010	3.950	1010010	4.750	1110010	5.550
0010011	3.175	0110011	3.975	1010011	4.775	1110011	5.575
0010100	3.200	0110100	4.000	1010100	4.800	1110100	5.600
0010101	3.225	0110101	4.025	1010101	4.825	1110101	5.625
0010110	3.250	0110110	4.050	1010110	4.850	1110110	5.650
0010111	3.275	0110111	4.075	1010111	4.875	1110111	5.675
0011000	3.300	0111000	4.100	1011000	4.900	1111000	5.700
0011001	3.325	0111001	4.125	1011001	4.925	1111001	5.725
0011010	3.350	0111010	4.150	1011010	4.950	1111010	5.750
0011011	3.375	0111011	4.175	1011011	4.975	1111011	5.775
0011100	3.400	0111100	4.200	1011100	5.000	1111100	5.800
0011101	3.425	0111101	4.225	1011101	5.025	1111101	5.825
0011110	3.450	0111110	4.250	1011110	5.050	1111110	5.850
0011111	3.475	0111111	4.275	1011111	5.075	1111111	5.875

VML [6:0] : Set the VCOML voltage

VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)
0000000	-2.500	0100000	-1.700	1000000	-0.900	1100000	-0.100
0000001	-2.475	0100001	-1.675	1000001	-0.875	1100001	-0.075
0000010	-2.450	0100010	-1.650	1000010	-0.850	1100010	-0.050
0000011	-2.425	0100011	-1.625	1000011	-0.825	1100011	-0.025
0000100	-2.400	0100100	-1.600	1000100	-0.800	1100100	0
0000101	-2.375	0100101	-1.575	1000101	-0.775	1100101	Reserved
0000110	-2.350	0100110	-1.550	1000110	-0.750	1100110	Reserved
0000111	-2.325	0100111	-1.525	1000111	-0.725	1100111	Reserved
0001000	-2.300	0101000	-1.500	1001000	-0.700	1101000	Reserved
0001001	-2.275	0101001	-1.475	1001001	-0.675	1101001	Reserved
0001010	-2.250	0101010	-1.450	1001010	-0.650	1101010	Reserved
0001011	-2.225	0101011	-1.425	1001011	-0.625	1101011	Reserved
0001100	-2.200	0101100	-1.400	1001100	-0.600	1101100	Reserved
0001101	-2.175	0101101	-1.375	1001101	-0.575	1101101	Reserved
0001110	-2.150	0101110	-1.350	1001110	-0.550	1101110	Reserved
0001111	-2.125	0101111	-1.325	1001111	-0.525	1101111	Reserved
0010000	-2.100	0110000	-1.300	1010000	-0.500	1110000	Reserved
0010001	-2.075	0110001	-1.275	1010001	-0.475	1110001	Reserved
0010010	-2.050	0110010	-1.250	1010010	-0.450	1110010	Reserved
0010011	-2.025	0110011	-1.225	1010011	-0.425	1110011	Reserved

0010100	-2.000	0110100	-1.200	1010100	-0.400	1110100	Reserved
0010101	-1.975	0110101	-1.175	1010101	-0.375	1110101	Reserved
0010110	-1.950	0110110	-1.150	1010110	-0.350	1110110	Reserved
0010111	-1.925	0110111	-1.125	1010111	-0.325	1110111	Reserved
0011000	-1.900	0111000	-1.100	1011000	-0.300	1111000	Reserved
0011001	-1.875	0111001	-1.075	1011001	-0.275	1111001	Reserved
0011010	-1.850	0111010	-1.050	1011010	-0.250	1111010	Reserved
0011011	-1.825	0111011	-1.025	1011011	-0.225	1111011	Reserved
0011100	-1.800	0111100	-1.000	1011100	-0.200	1111100	Reserved
0011101	-1.775	0111101	-0.975	1011101	-0.175	1111101	Reserved
0011110	-1.750	0111110	-0.950	1011110	-0.150	1111110	Reserved
0011111	-1.725	0111111	-0.925	1011111	-0.125	1111111	Reserved

Restriction: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	VMH [6:0]	VML [6:0]
Power ON Sequence	7'h31	7'h3C
SW Reset	7'h31	7'h3C
HW Rest	7'h31	7'h3C

8.3.17. VCOM Control 2(C7h)

C7h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
Parameter	1	1	↑	XX	nVM	VMF [6:0]							C0

Description

nVM: nVM equals to “0” after power on reset and VCOM offset equals to program MTP value. When nVM set to “1”, setting of VMF [6:0] becomes valid and VCOMH/VCOML can be adjusted.

VMF [6:0]: Set the VCOM offset voltage.

VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML
0000000	VMH	VML	1000000	VMH	VML
0000001	VMH – 63	VML – 63	1000001	VMH + 1	VML + 1
0000010	VMH – 62	VML – 62	1000010	VMH + 2	VML + 2
0000011	VMH – 61	VML – 61	1000011	VMH + 3	VML + 3
0000100	VMH – 60	VML – 60	1000100	VMH + 4	VML + 4
0000101	VMH – 58	VML – 58	1000101	VMH + 5	VML + 5
0000110	VMH – 58	VML – 58	1000110	VMH + 6	VML + 6
0000111	VMH – 57	VML – 57	1000111	VMH + 7	VML + 7
0001000	VMH – 56	VML – 56	1001000	VMH + 8	VML + 8
0001001	VMH – 55	VML – 55	1001001	VMH + 9	VML + 9
0001010	VMH – 54	VML – 54	1001010	VMH + 10	VML + 10
0001011	VMH – 53	VML – 53	1001011	VMH + 11	VML + 11
0001100	VMH – 52	VML – 52	1001100	VMH + 12	VML + 12
0001101	VMH – 51	VML -51	1001101	VMH + 13	VML + 13
0001110	VMH – 50	VML – 50	1001110	VMH + 14	VML + 14
0001111	VMH – 49	VML – 49	1001111	VMH + 15	VML + 15
0010000	VMH – 48	VML – 48	1010000	VMH + 16	VML + 16
0010001	VMH – 47	VML – 47	1010001	VMH + 17	VML + 17
0010010	VMH – 46	VML – 46	1010010	VMH + 18	VML + 18
0010011	VMH – 45	VML – 45	1010011	VMH + 19	VML + 19
0010100	VMH – 44	VML – 44	1010100	VMH + 20	VML + 20
0010101	VMH – 43	VML – 43	1010101	VMH + 21	VML + 21
0010110	VMH – 42	VML – 42	1010110	VMH + 22	VML + 22
0010111	VMH – 41	VML – 41	1010111	VMH + 23	VML + 23
0011000	VMH – 40	VML – 40	1011000	VMH + 24	VML + 24
0011001	VMH – 39	VML – 39	1011001	VMH + 25	VML + 25
0011010	VMH – 38	VML – 38	1011010	VMH + 26	VML + 26
0011011	VMH – 37	VML – 37	1011011	VMH + 27	VML + 27
0011100	VMH – 36	VML – 36	1011100	VMH + 28	VML + 28
0011101	VMH – 35	VML – 35	1011101	VMH + 29	VML + 29
0011110	VMH – 34	VML – 34	1011110	VMH + 30	VML + 30
0011111	VMH – 33	VML – 33	1011111	VMH + 31	VML + 31
0100000	VMH – 32	VML – 32	1100000	VMH + 32	VML + 32
0100001	VMH – 31	VML – 31	1100001	VMH + 33	VML + 33
0100010	VMH – 30	VML – 30	1100010	VMH + 34	VML + 34
0100011	VMH – 29	VML – 29	1100011	VMH + 35	VML + 35
0100100	VMH – 28	VML – 28	1100100	VMH + 36	VML + 36
0100101	VMH – 27	VML – 27	1100101	VMH + 37	VML + 37
0100110	VMH – 26	VML – 26	1100110	VMH + 38	VML + 38
0100111	VMH – 25	VML – 25	1100111	VMH + 39	VML + 39
0101000	VMH – 24	VML – 24	1101000	VMH + 40	VML + 40
0101001	VMH – 23	VML – 23	1101001	VMH + 41	VML + 41
0101010	VMH – 22	VML – 22	1101010	VMH + 42	VML + 42
0101011	VMH – 21	VML – 21	1101011	VMH + 43	VML + 43
0101100	VMH – 20	VML – 20	1101100	VMH + 44	VML + 44
0101101	VMH – 19	VML – 19	1101101	VMH + 45	VML + 45
0101110	VMH – 18	VML – 18	1101110	VMH + 46	VML + 46
0101111	VMH – 17	VML – 17	1101111	VMH + 47	VML + 47
0110000	VMH – 16	VML – 16	1110000	VMH + 48	VML + 48
0110001	VMH – 15	VML – 15	1110001	VMH + 49	VML + 49
0110010	VMH – 14	VML – 14	1110010	VMH + 50	VML + 50
0110011	VMH – 13	VML – 13	1110011	VMH + 51	VML + 51

	0110100	VMH – 12	VML – 12	1110100	VMH + 52	VML + 52
	0110101	VMH – 11	VML – 11	1110101	VMH + 53	VML + 53
	0110110	VMH – 10	VML – 10	1110110	VMH + 54	VML + 54
	0110111	VMH – 9	VML – 9	1110111	VMH + 55	VML + 55
	0111000	VMH – 8	VML – 8	1111000	VMH + 56	VML + 56
	0111001	VMH – 7	VML – 7	1111001	VMH + 57	VML + 57
	0111010	VMH – 6	VML – 6	1111010	VMH + 58	VML + 58
	0111011	VMH – 5	VML – 5	1111011	VMH + 59	VML + 59
	0111100	VMH – 4	VML – 4	1111100	VMH + 60	VML + 60
	0111101	VMH – 3	VML – 3	1111101	VMH + 61	VML + 61
	0111110	VMH – 2	VML – 2	1111110	VMH + 62	VML + 62
	0111111	VMH – 1	VML – 1	1111111	VMH + 63	VML + 63

Restriction	SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	nVM	VMF [6:0]
Power ON Sequence	1'b1	7'h40h
SW Reset	1'b1	7'h40h
HW Reset	1'b1	7'h40h

8.3.18. NV Memory Write (D0h)

<table>
<tr><th>D0h</th><th colspan="13">NVMWR (NV Memory Write)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">PGM_ADR [2:0]</td><td>00</td></tr>
<tr><td>2ndParameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="9">PGM_DATA [7:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to program the NV memory data. After a successful MTP operation, the information of PGM_DATA [7:0] will programmed to NV memory.
PGM_ADR [2:0]: The select bits of ID1, ID2, ID3 and VMF [6:0] programming.

<table>
<tr><th colspan="3">PGM_ADR [2:0]</th><th>Programmed NV Memory Selection</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>ID1 programming</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>ID2 programming</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID3 programming</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>VMF [6:0] programming</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table>

PGM_DATA [7:0]: The programmed data.</td></tr>
<tr><td>Restriction</td><td colspan="13">SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>PGM_ADR [2:0]</th><th>PGM_DATA [7:0]</th></tr>
<tr><td>Power ON Sequence</td><td>3’b000</td><td>MTP value</td></tr>
<tr><td>SW Reset</td><td>3’b000</td><td>MTP value</td></tr>
<tr><td>HW Reset</td><td>3’b000</td><td>MTP value</td></tr>
</table>
</td></tr>
</table>

8.3.19. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h
1st Parameter	1	1	↑	XX	KEY [23:16]								55h
2nd Parameter	1	1	↑	XX	KEY [15:8]								AAh
3rd Parameter	1	1	↑	XX	KEY [7:0]								66h
Description	**KEY [23:0]:** NV memory programming protection key. When writing MTP data to D1h, this register must be set to 0x55AA66h to enable MTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.												
Restriction	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	KEY [23:0]=55AA66h
SW Reset	KEY [23:0]=55AA66h
HW Reset	KEY [23:0]=55AA66h

8.3.20. NV Memory Status Read (D2h)

D2h	RDNVM (NV Memory Status Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	ID2_CNT [2:0]			0	ID1_CNT [2:0]			XX
3rd Parameter	1	↑	1	XX	BUSY	VMF_CNT [2:0]			0	ID3_CNT [2:0]			XX

Description

ID1_CNT [2:0] / ID2_CNT [2:0] / ID3_CNT [2:0] / VMF_CNT [2:0]: NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

ID1_CNT [2:0] / ID2_CNT [2:0] ID3_CNT [2:0] / VMF_CNT [2:0]			Description
Status			Availability
0	0	0	No Programmed
0	0	1	Programmed 1 time
0	1	1	Programmed 2 times
1	1	1	Programmed 3 times

BUSY: The status bit of NV memory programming.

BUSY	The Status of NV Memory
0	Idle
1	Busy

Restriction

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value				
	ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY
Power ON Sequence	X	X	X	X	X
SW Reset	X	X	X	X	X
HW Reset	X	X	X	X	X

8.3.21. Read ID4 (D3h)

D3h	RDID4 (Read ID4)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00h
3rdParameter	1	↑	1	XX	1	0	0	1	0	0	1	1	93h
4th Parameter	1	↑	1	XX	0	1	0	0	0	0	1	0	42h
Description	Read IC device code. The 1st parameter is dummy read period. The 2nd parameter means the IC version. The 3rd and 4th parameter mean the IC model name.												
Restriction	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	24'h009342h
SW Reset	24'h009342h
HW Reset	24'h009342h

8.3.22. Positive Gamma Correction (E0h)

E0h	PGAMCTRL (Positive Gamma Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
1st Parameter	1	1	↑	XX	0	0	0	VP0 [4:0]					00
2ndParameter	1	1	↑	XX	0	0	VP1 [5:0]						0E
3rdParameter	1	1	↑	XX	0	0	VP2 [5:0]						13
4th Parameter	1	1	↑	X	0	0	0	0	VP4 [3:0]				04
5th Parameter	1	1	↑	XX	0	0	0	VP6 [4:0]					1C
6th Parameter	1	1	↑	XX	0	0	0	0	VP13 [3:0]				03
7th Parameter	1	1	↑	XX	0	VP20 [6:0]							3D
8th Parameter	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]				74
9th Parameter	1	1	↑	XX	0	VP43 [6:0]							49
10thParameter	1	1	↑	XX	0	0	0	0	VP50 [3:0]				03
11thParameter	1	1	↑	XX	0	0	0	VP57 [4:0]					0C
12thParameter	1	1	↑	XX	0	0	0	0	VP59 [3:0]				05
13thParameter	1	1	↑	XX	0	0	VP61 [5:0]						1B
14thParameter	1	1	↑	XX	0	0	VP62 [5:0]						22
15thParameter	1	1	↑	XX	0	0	0	VP63 [4:0]					0F
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	SETEXTC turn on to enable this command.												
Register Availability													
Default													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

8.3.23. Negative Gamma Correction (E1h)

E1h	NGAMCTRL (Negative Gamma Correction)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h
1st Parameter	1	1	↑	XX	0	0	0	VN0 [4:0]					00
2ndParameter	1	1	↑	XX	0	0	VN1 [5:0]						23
3rdParameter	1	1	↑	XX	0	0	VN2 [5:0]						26
4th Parameter	1	1	↑	XX	0	0	0	0	VN4 [3:0]				05
5th Parameter	1	1	↑	XX	0	0	0	VN6 [4:0]					10
6th Parameter	1	1	↑	XX	0	0	0	0	VN13 [3:0]				04
7th Parameter	1	1	↑	XX	0	VN20 [6:0]							39
8th Parameter	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]				24
9th Parameter	1	1	↑	XX	0	VN43 [6:0]							4B
10thParameter	1	1	↑	XX	0	0	0	0	VN50 [3:0]				03
11thParameter	1	1	↑	XX	0	0	0	VN57 [4:0]					0B
12thParameter	1	1	↑	XX	0	0	0	0	VN59 [3:0]				0B
13thParameter	1	1	↑	XX	0	0	VN61 [5:0]						33
14thParameter	1	1	↑	XX	0	0	VN62 [5:0]						37
15thParameter	1	1	↑	XX	0	0	0	VN63 [4:0]					0F
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	SETEXTC turn on to enable this command.												
Register Availability													
Default													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

8.3.24. Digital Gamma Control 1 (E2h)

E2h	DGAMCTRL (Digital Gamma Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				XX
:	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				XX
16th Parameter	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]				XX
Description	**RCAx [3:0]:** Gamma Macro-adjustment registers for red gamma curve. **BCAx [3:0]:** Gamma Macro-adjustment registers for blue gamma curve.												
Restriction	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	RCAx [3:0]	BCAx [3:0]
Power ON Sequence	TBD	TBD
SW Reset	TBD	TBD
HW Reset	TBD	TBD

8.3.25. Digital Gamma Control 2(E3h)

E3h	DGAMCTRL (Digital Gamma Control 2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1st Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				XX
:	1	1	↑	XX	RFAx [3:0]				BFAx [3:0]				XX
64rdParameter	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]				XX
Description	**RFAx [3:0]:** Gamma Micro-adjustment registers for red gamma curve. **BFAx [3:0]:** Gamma Micro-adjustment registers for blue gamma curve.												
Restriction	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	RFAx [3:0]	BFAx [3:0]
Power ON Sequence	TBD	TBD
SW Reset	TBD	TBD
HW Reset	TBD	TBD

8.3.26. Interface Control (F6h)

F6h	IFCTL (16bits Data Format Selection)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
1st Parameter	1	1	↑	XX	MY_ EOR	MX_ EOR	MV_ EOR	0	BGR_ EOR	0	0	WE MODE	01
2nd Parameter	1	1	↑	XX	0	0	EPF [1:0]		0	0	0	0	00
3rd Parameter	1	1	↑	XX	0	0	ENDIAN	0	DM [1:0]		RM	RIM	00

Description

MY_EOR / MX_EOR / MV_EOR / BGR_EOR:

The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

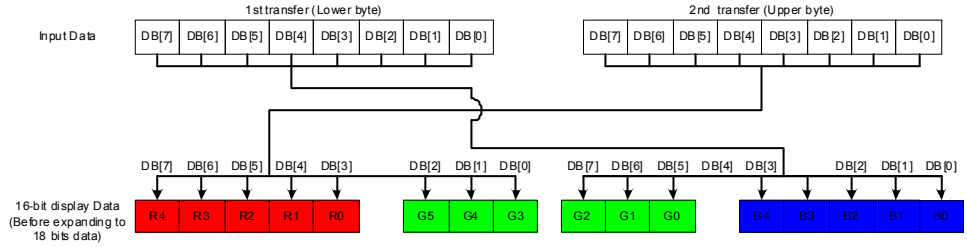
WEMODE: Memory write control

WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

ENDIAN	Data transfer Mode
0	Normal (MSB first, default)
1	Little Endian (LSB first)



Note: Little Endian is valid on only 65K 8-bit and 9-bit MPU interface mode.

DM [1:0]: Select the display operation mode.

DM [1]	DM [0]	Display Operation Mode
0	0	Internal clock operation
0	1	RGB Interface Mode
1	0	VSYNC interface mode
1	1	Setting disabled

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM: Select the interface to access the GRAM.

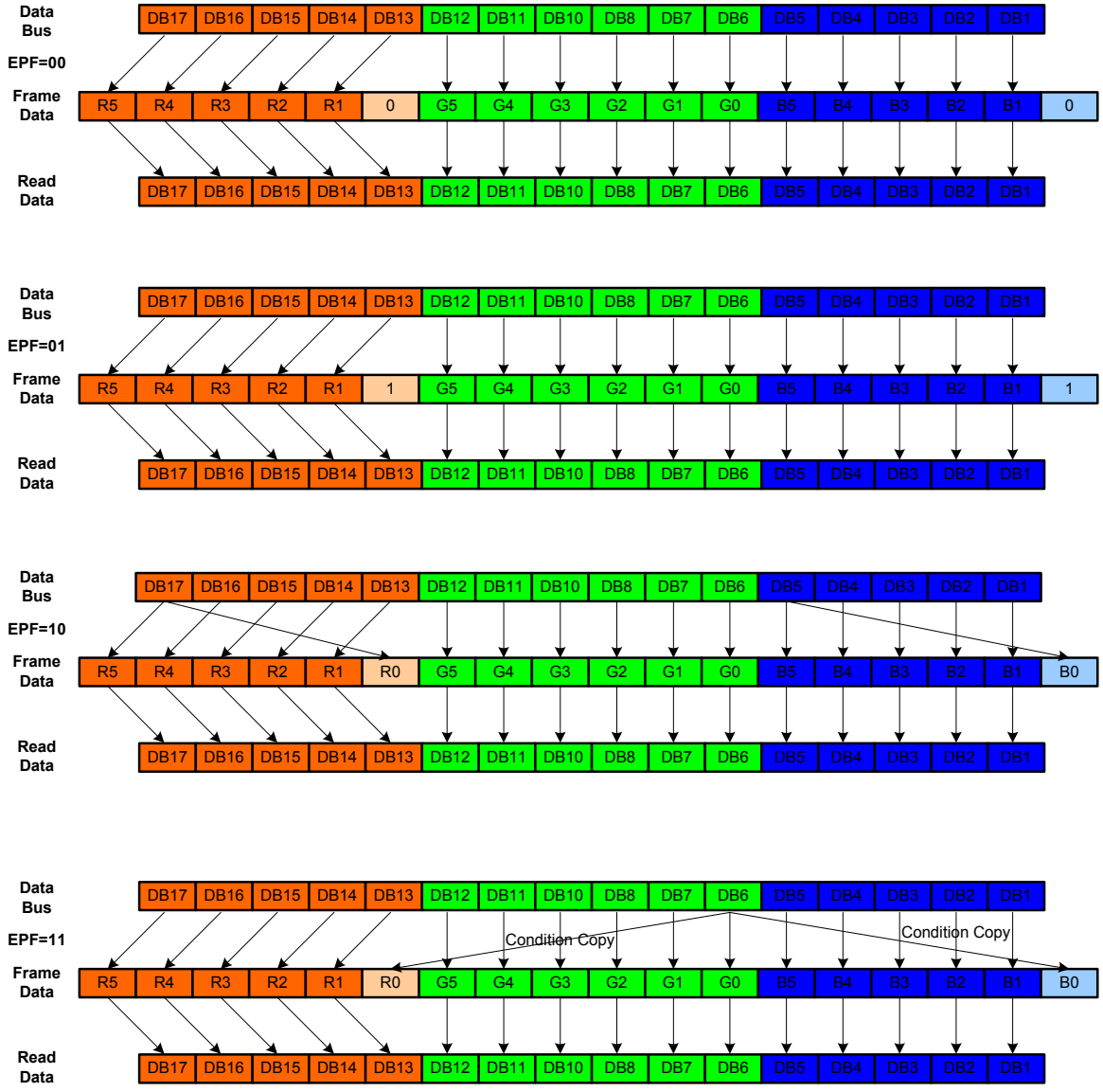
Set RM to "1" when writing display data by the RGB interface.

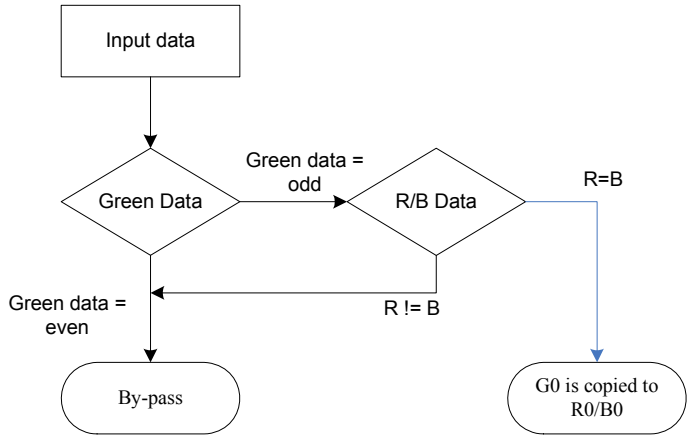
RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]: 65K color mode data format.





EPF [1:0]	Expand 16 bbp (R,G,B) to 18bbp (R,G,B)
00	MSB is inputted to LSB r [5:0] = {R [4:0], R [4]} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], B [4]}
01	"0" is inputted to LSB r [5:0] = {R [4:0], 0} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 0} Exception: R [4:0], B[4:0] = 5'h1F → r [5:0], b[5:0] = 6'h3F
10	"1" is inputted to LSB r [5:0] = {R [4:0], 1} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 1} Exception: R [4:0], B[4:0] = 5'h00 → r [5:0], b[5:0] = 6'h00
11	Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]} Case 2: R=B≠G → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 3: R=G≠B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]}

Restriction

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value					
	EPF [1:0]	ENDIAN	WEMODE	DM [1:0]	RM	RIM
Power ON Sequence	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0
SW Reset	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0
HW Reset	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0

8.3.27. Get GPIO0~7 Status (F7h)

F7h	Get GPIO0~7 Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	1	F7h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	GPI[7:0]								00
Description	**GPI[7:0]:** get the GPIO0~7 input configuration correspondent with register GPI bit 0 ~ 7. 0 : logic low input 1 : logic High input												
Restriction	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
	GPI[7:0]
Power ON Sequence	7'h00h
SW Reset	7'h00h
HW Reset	7'h00h

8.3.28. Set GPIO0~7 Status (F8h)

F8h	Set GPIO0~7 Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	0	0	0	F8h
1st Parameter	1	1	↑	XX	GPO[7:0]								00
2ndParameter	1	1	↑	XX							IE	OEB	00
Description	**GPO[7:0] :** Setting the GPIO output configuration 0 : GPIO output is logic low 1 : GPIO output is logic High **IE/OEB :** Control the GPO output direction												
Restriction	SETEXTC turn on to enable this command.												

IE	OEB	GPO output control
0	0	Enable GPIO output
1	1	Disable GPIO output

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

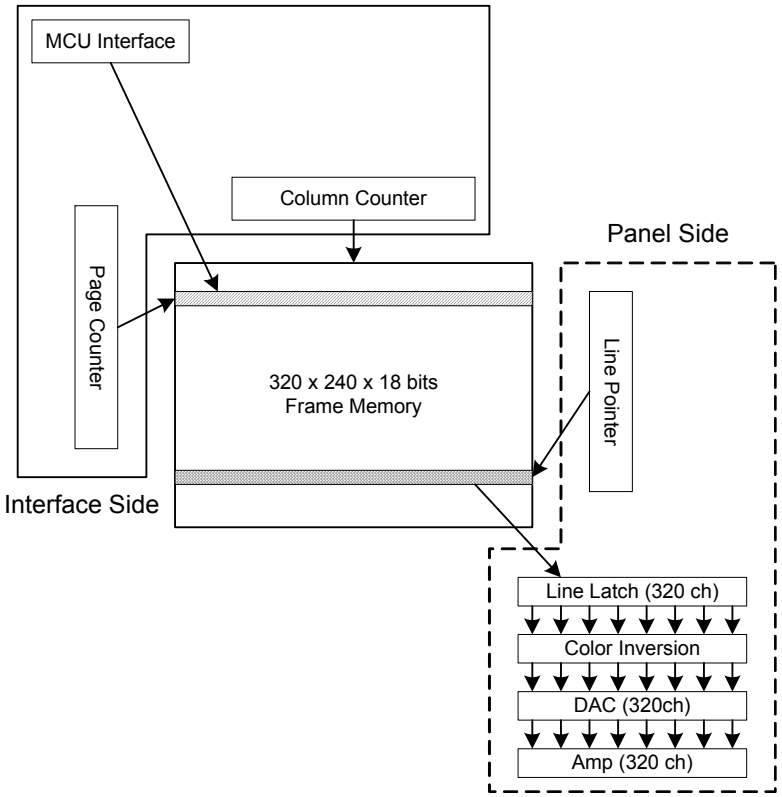
Default

Status	Default Value		
	GPO[7:0]	IE	OEB
Power ON Sequence	7'h00h	1'b0	1'b0
SW Reset	7'h00h	1'b0	1'b0
HW Reset	7'h00h	1'b0	1'b0

9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (320x18x240 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

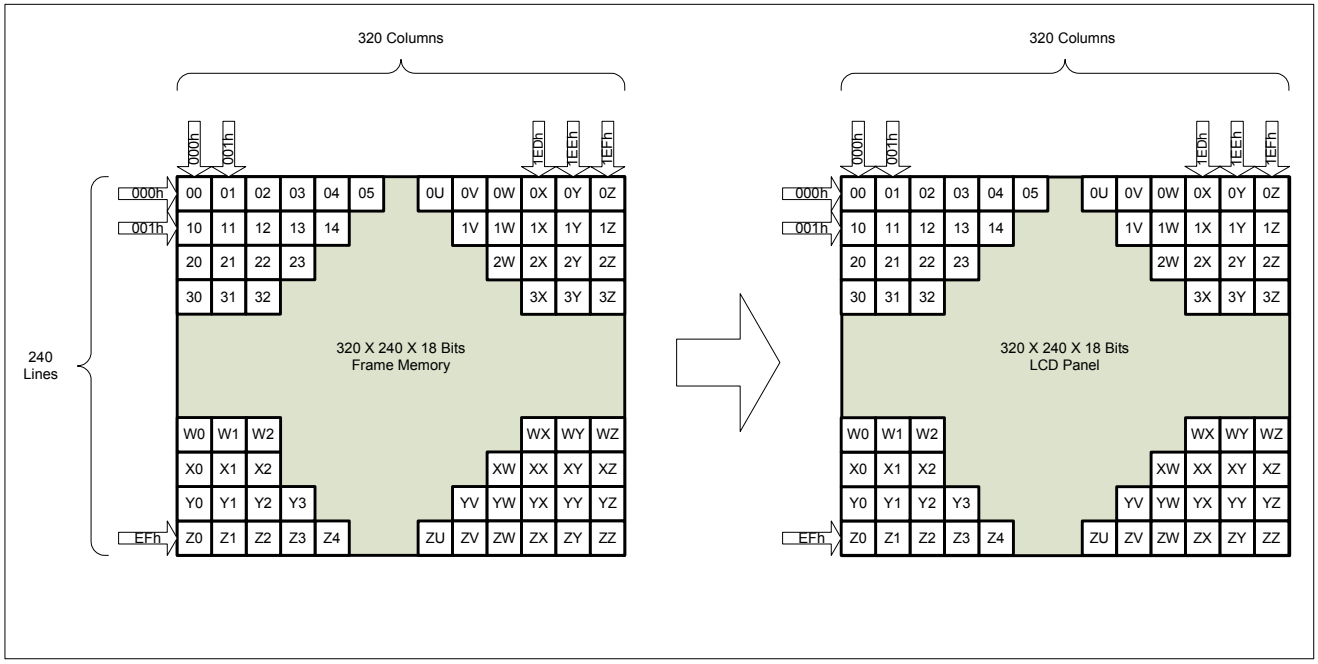


9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 00EFh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

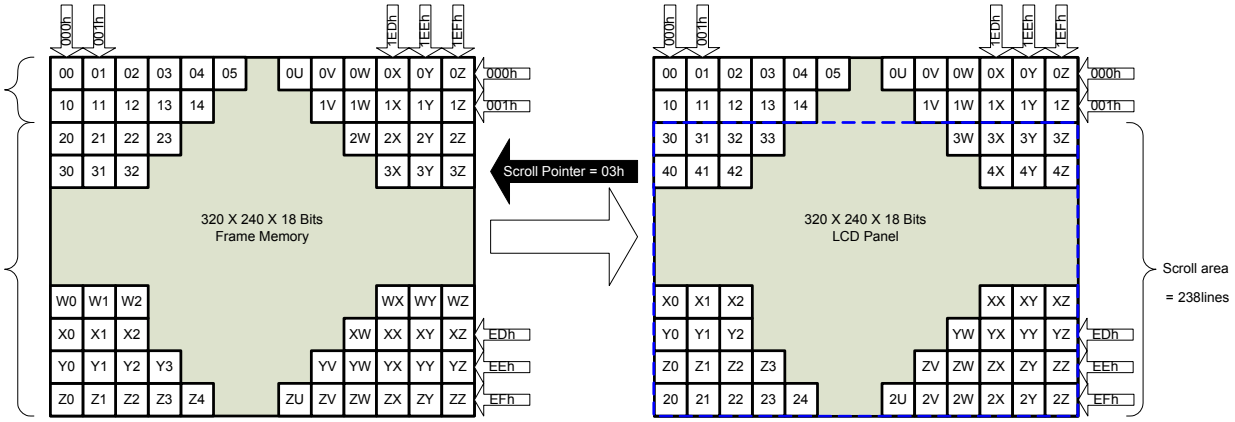


9.2.2. Vertical Scroll Mode

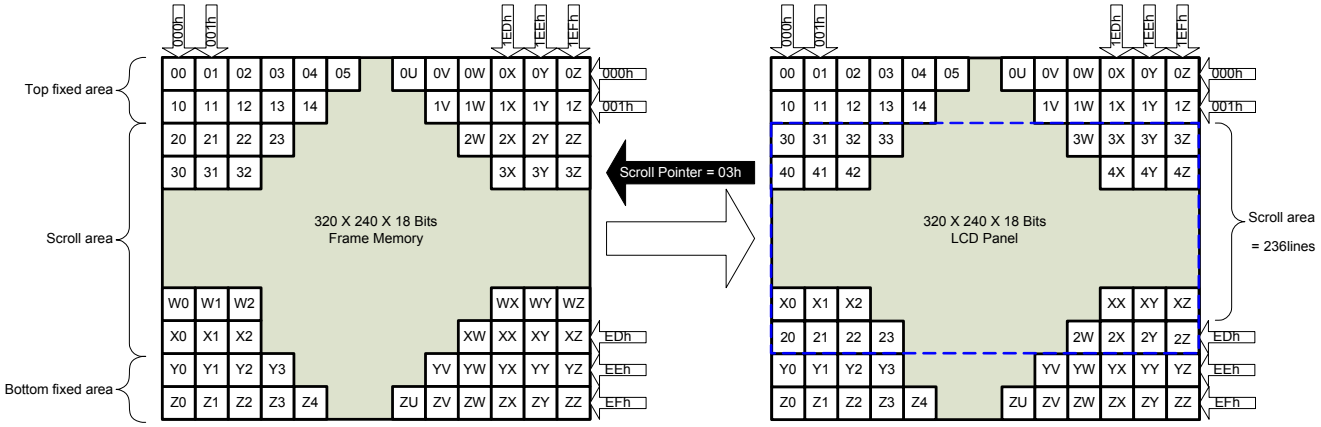
There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.

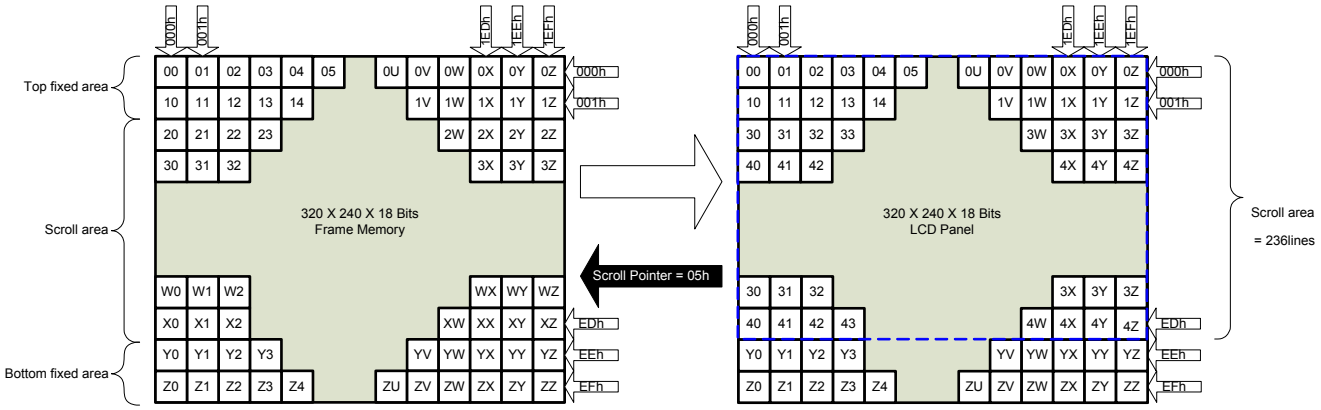
TFA=2, VSA=238, BFA=0 when MADCTL MV bit = 0



TFA=2, VSA=236, BFA=2 when MADCTL MV bit = 0



TFA=0, VSA=236, BFA=4 when MADCTL MV bit = 0



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 240, Scrolling Mode is undefined.

9.2.3. Vertical Scroll Example

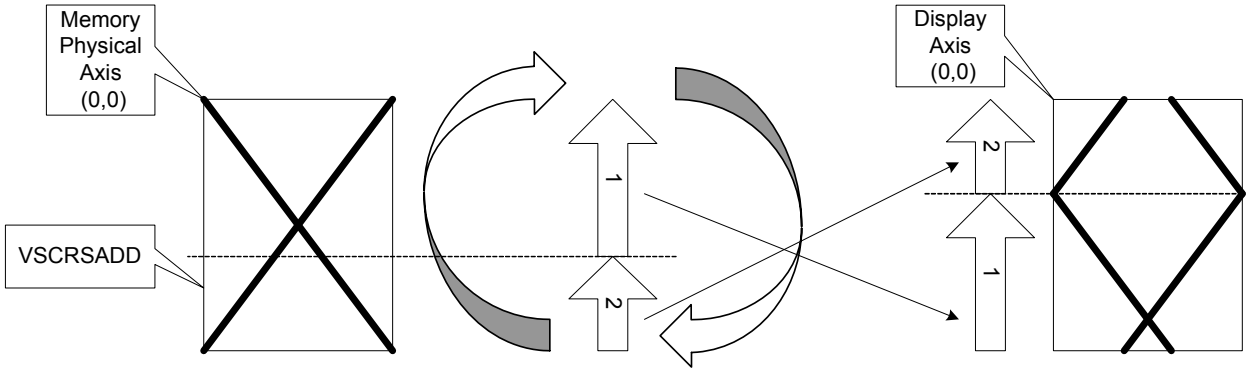
9.2.4. Case1: TFA+VSA+BFA < 240

This setting is prohibited, unless unexpected picture will be shown.

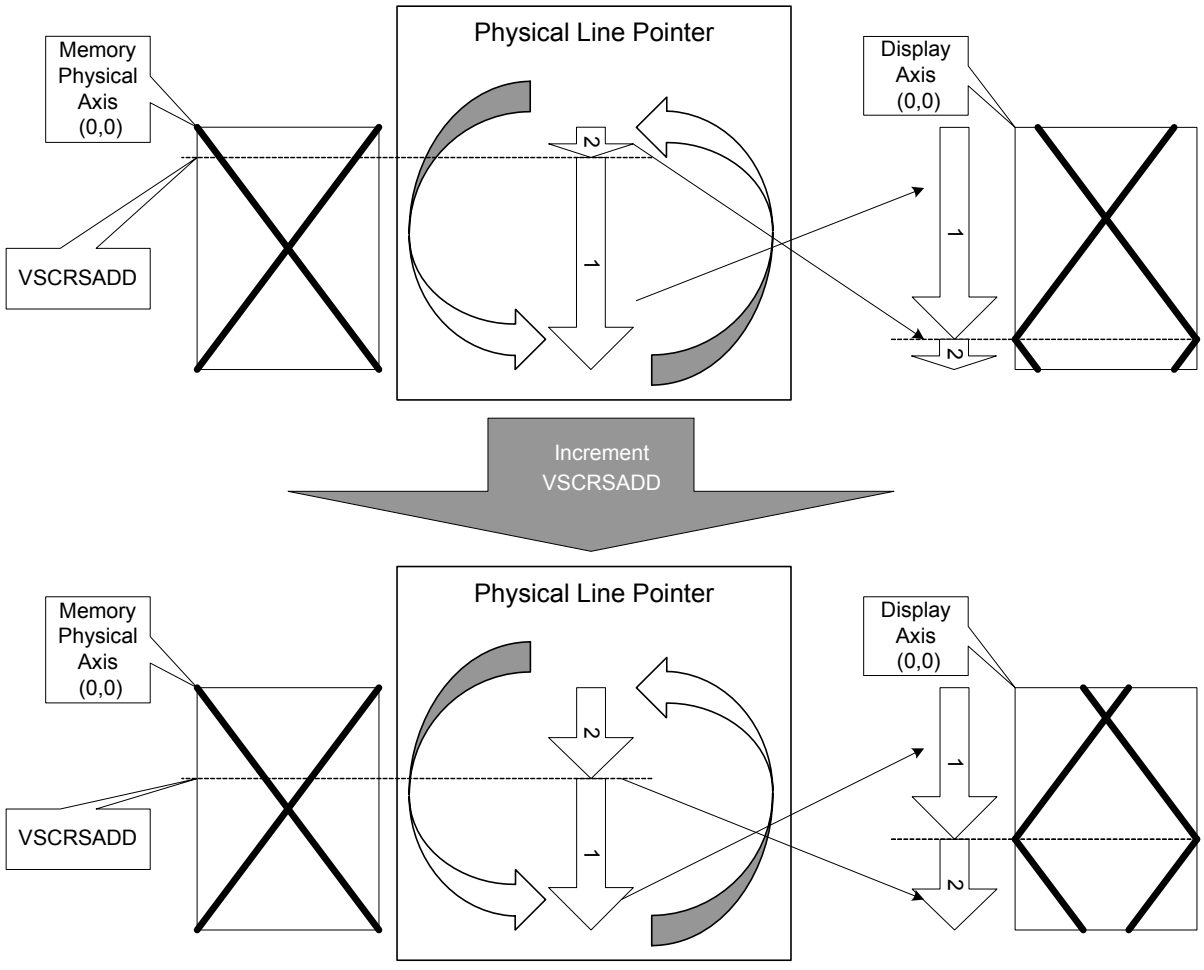
9.2.5. Case2: TFA+VSA+BFA = 240 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

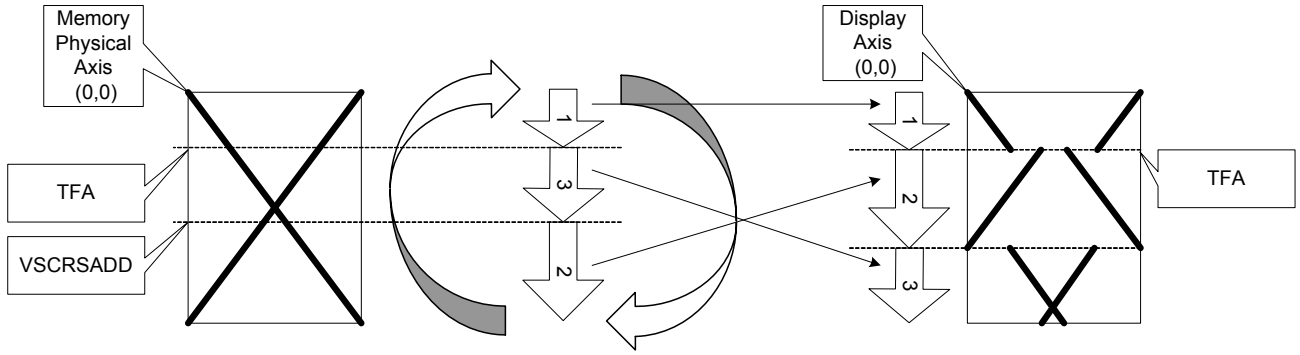
When TFA=0, VSA=240, BFA=0, VSCRSADD=40 and MADCTL MV bit = 1



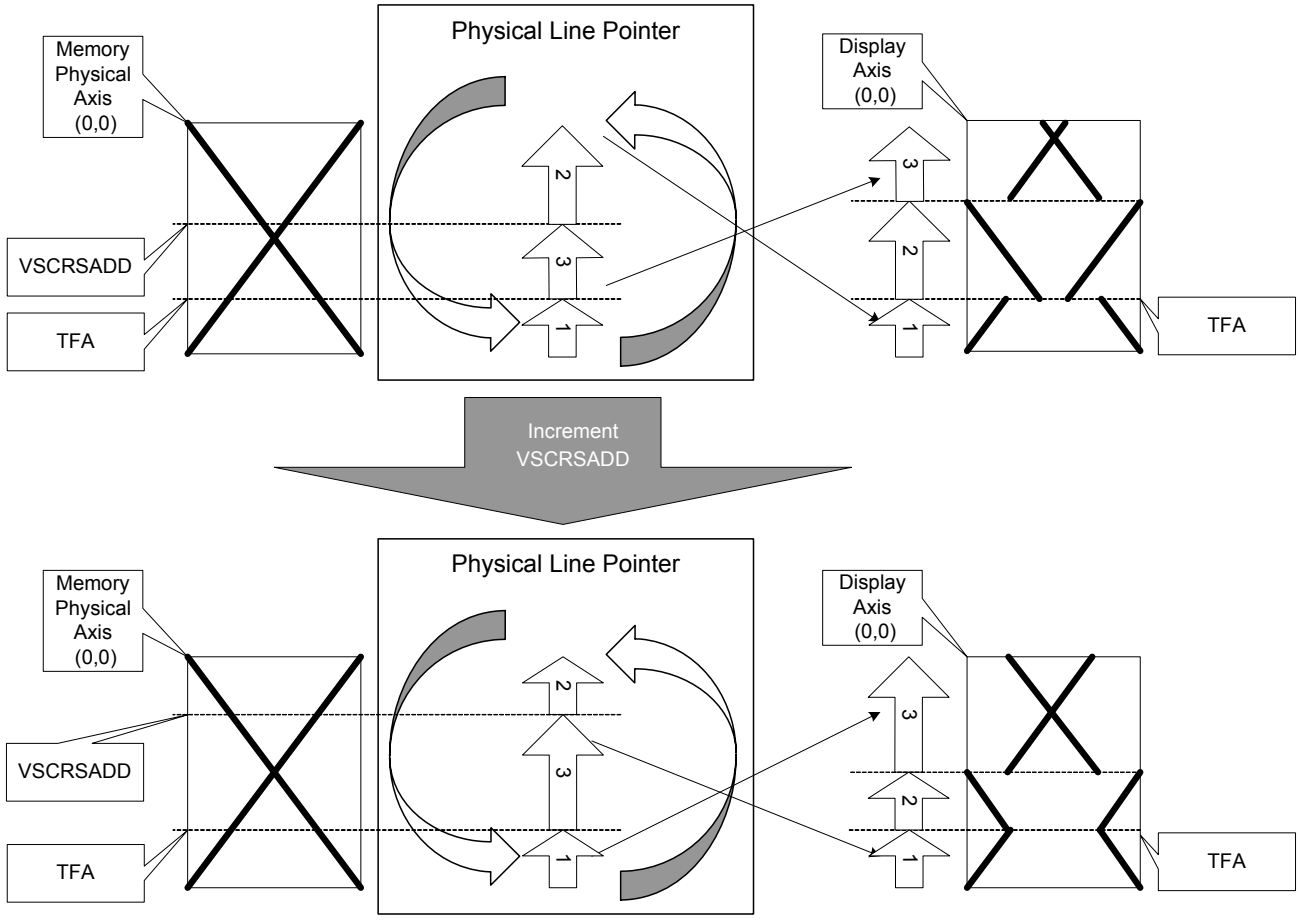
When TFA=0, VSA=240, BFA=0, VSCRSADD=40 and MADCTL MV bit = 0



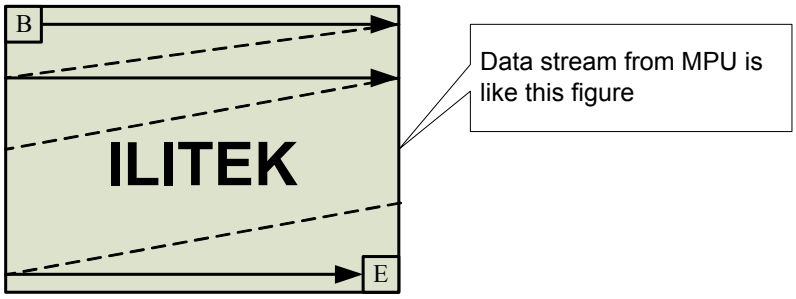
When TFA=30, VSA=210, BFA=0, VSCRSADD=80 and MADCTL MV bit = 0



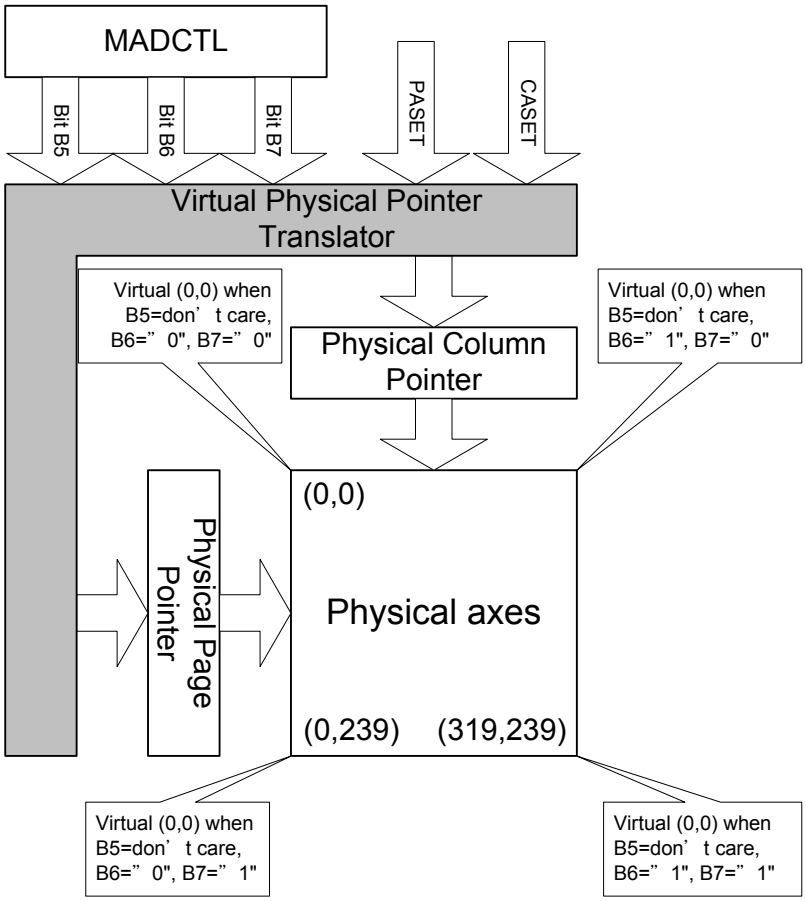
When TFA=30, VSA=210, BFA=0, VSCRSADD=80 and MADCTL MV bit = 1



9.3. MPU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (239-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (239-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (239-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (239-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

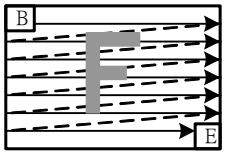
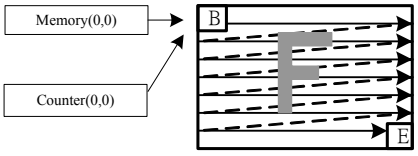
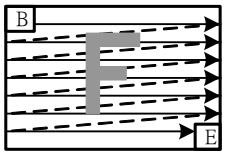
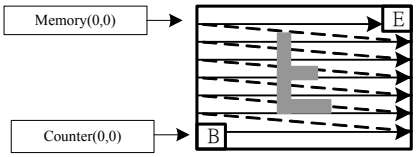
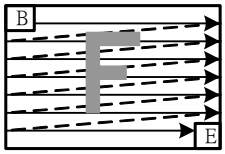
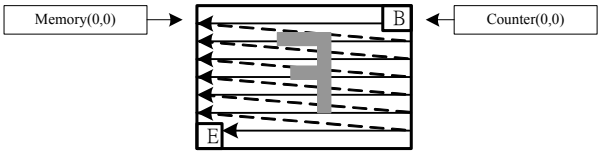
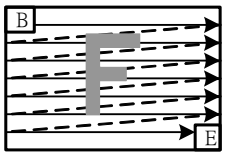
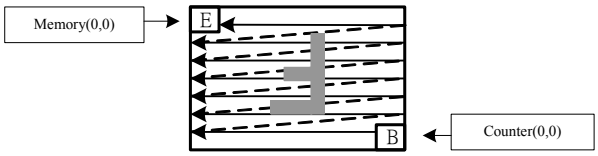
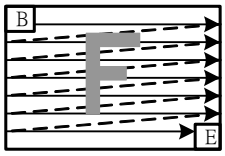
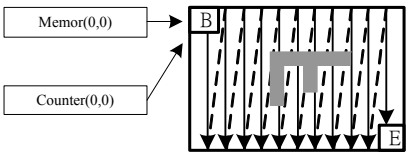
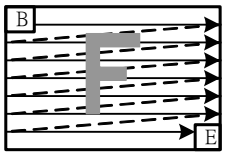
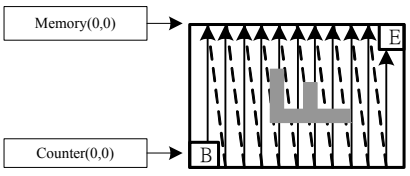
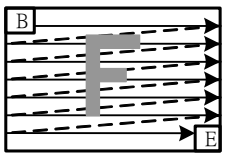
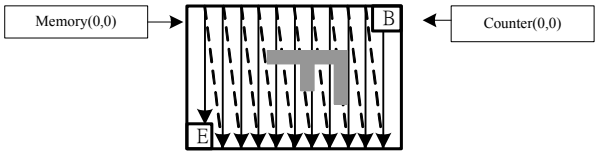
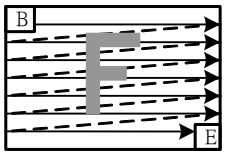
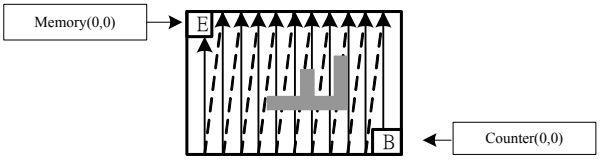
Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange X-Mirror	1	1	0		
XY Exchange X-Mirror Y-Mirror	1	1	1		

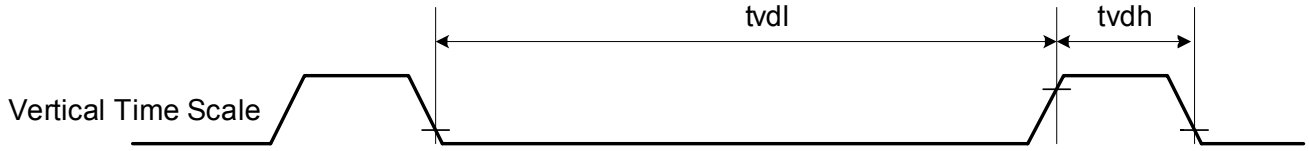
10. Tearing Effect Output

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

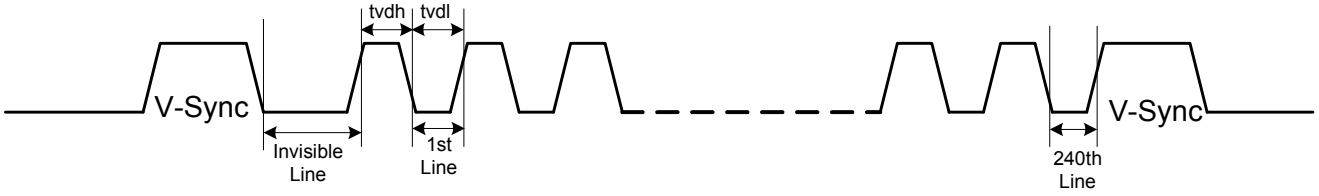
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

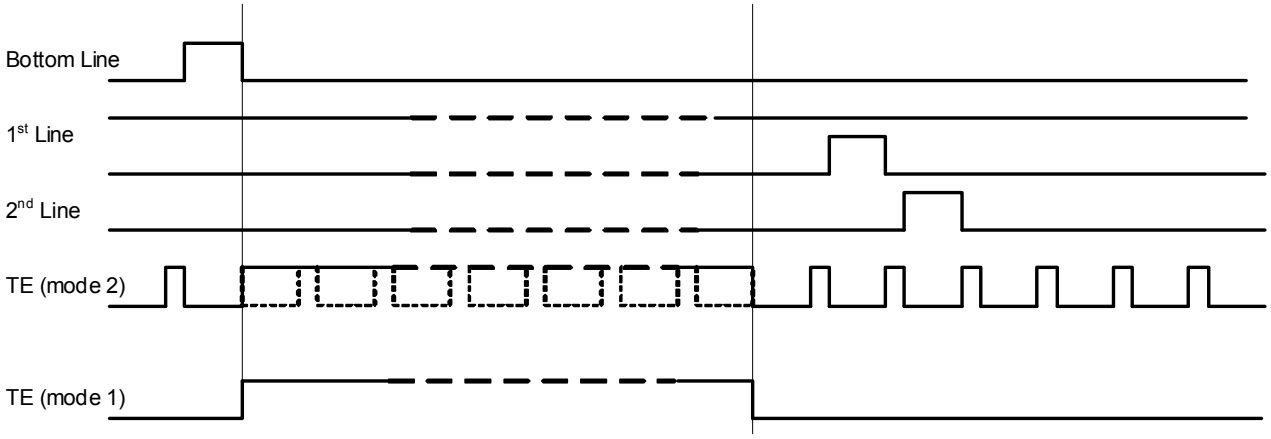
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 240 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

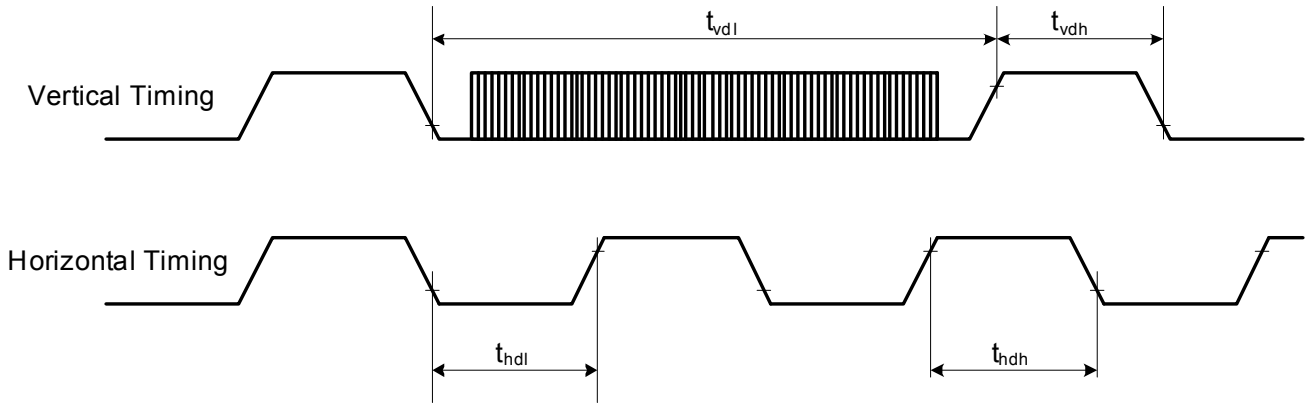
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

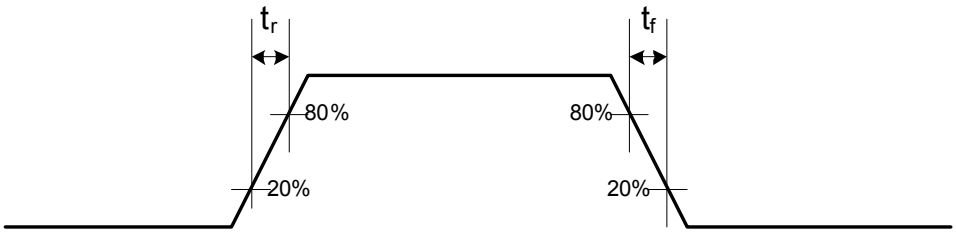


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	--	--	--	ms	
t_{vdh}	Vertical timing high duration	1000	--	--	us	
t_{hdl}	Horizontal timing low duration	--	--	--	us	
t_{hdh}	Horizontal timing high duration	--	--	500	us	

Note:

1. The timings in Table as above apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MPU and should be used to avoid Tearing Effect.

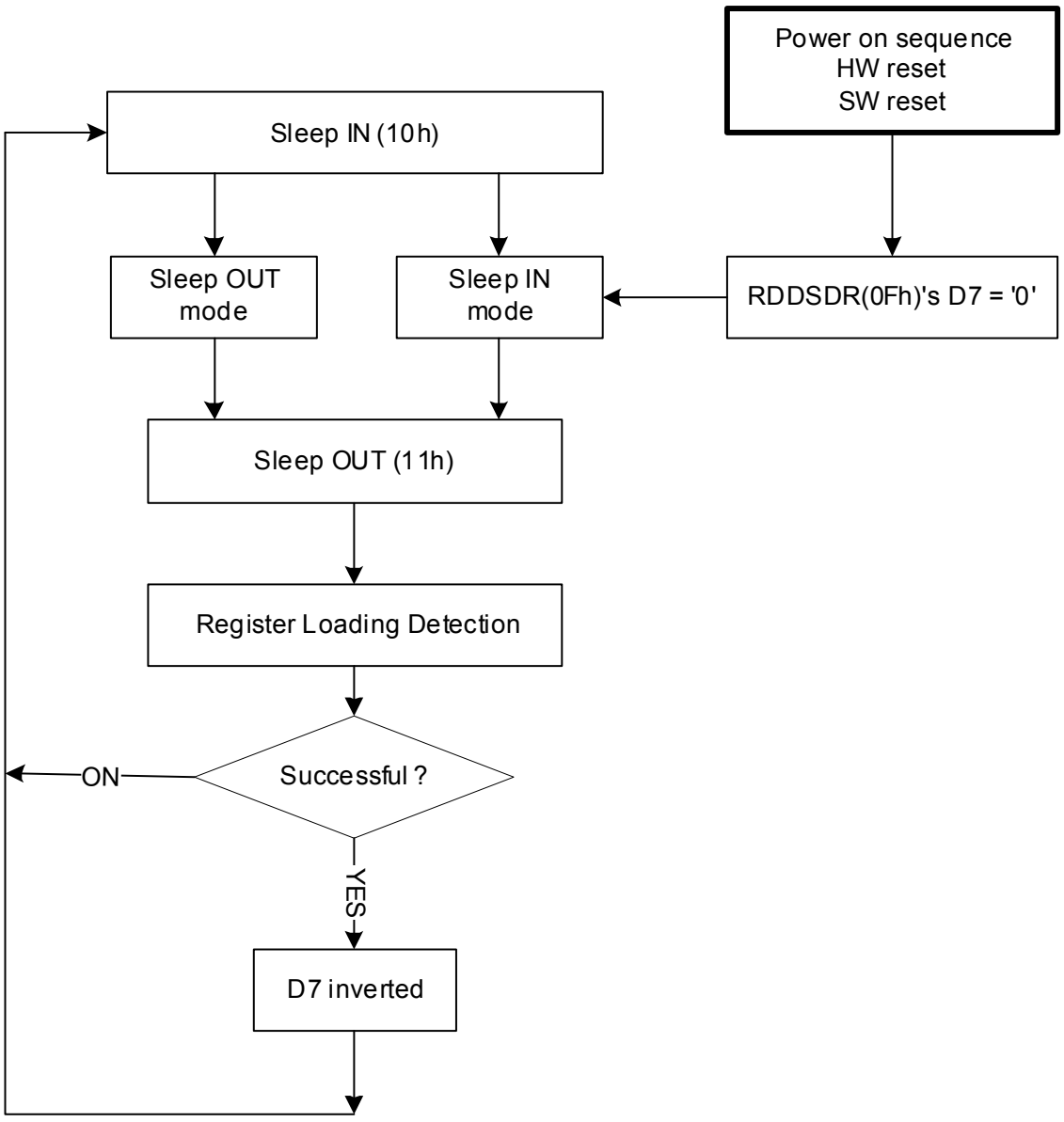
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

11.1. Register loading Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

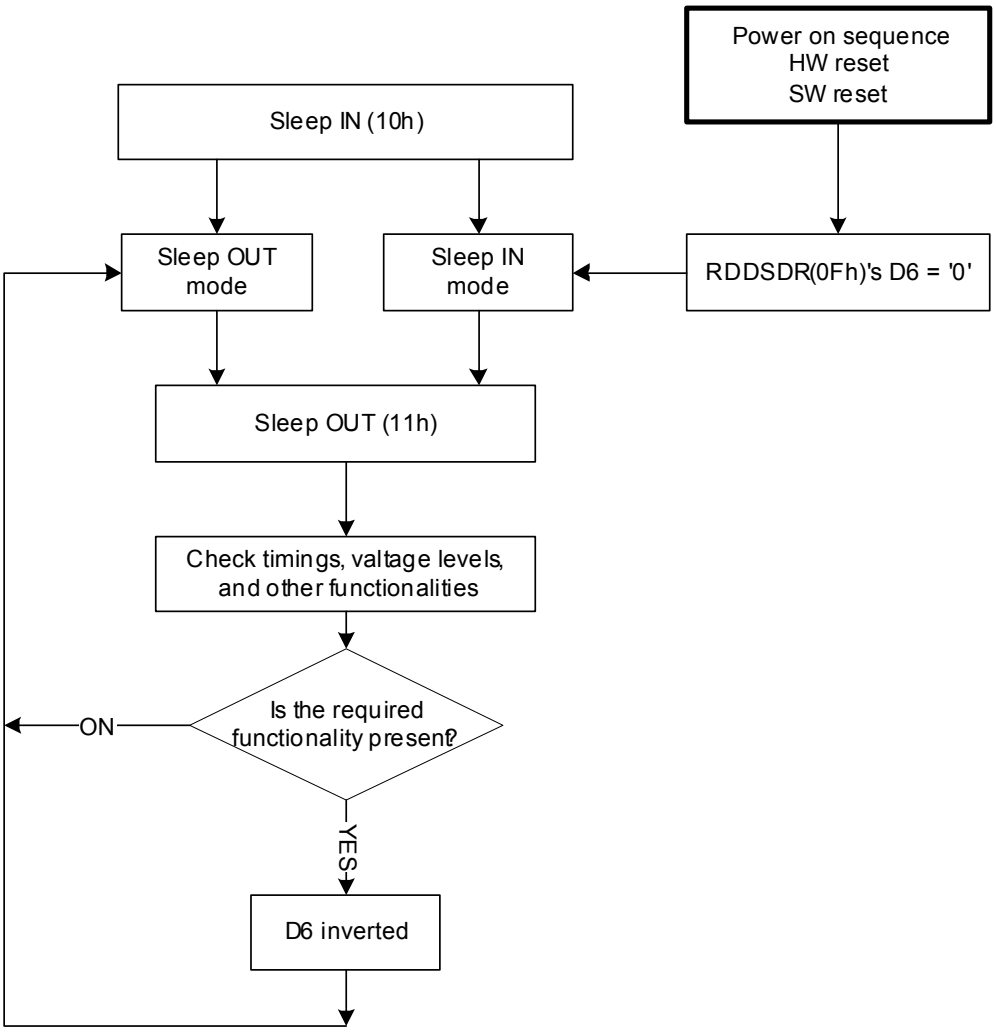


11.2. Functionality Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

12. Power ON/OFF Sequence

IOVCC and VCI can be applied in any order.

VCI and IOVCC can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

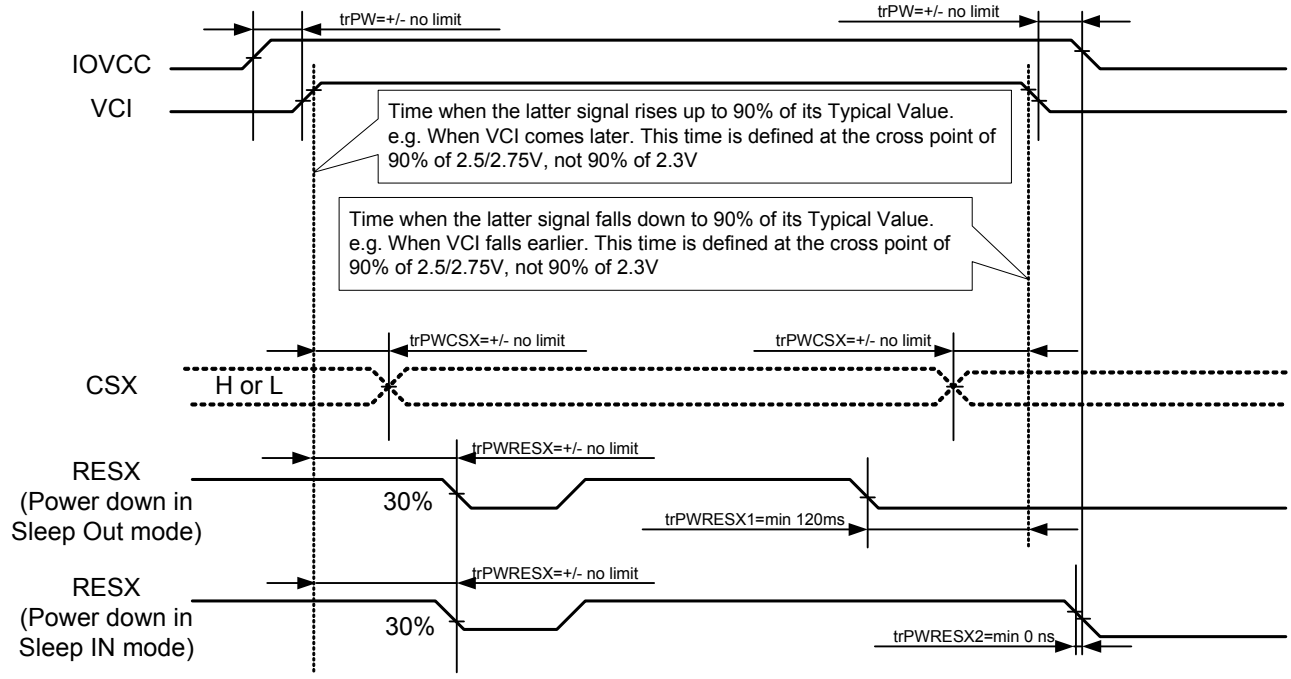
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

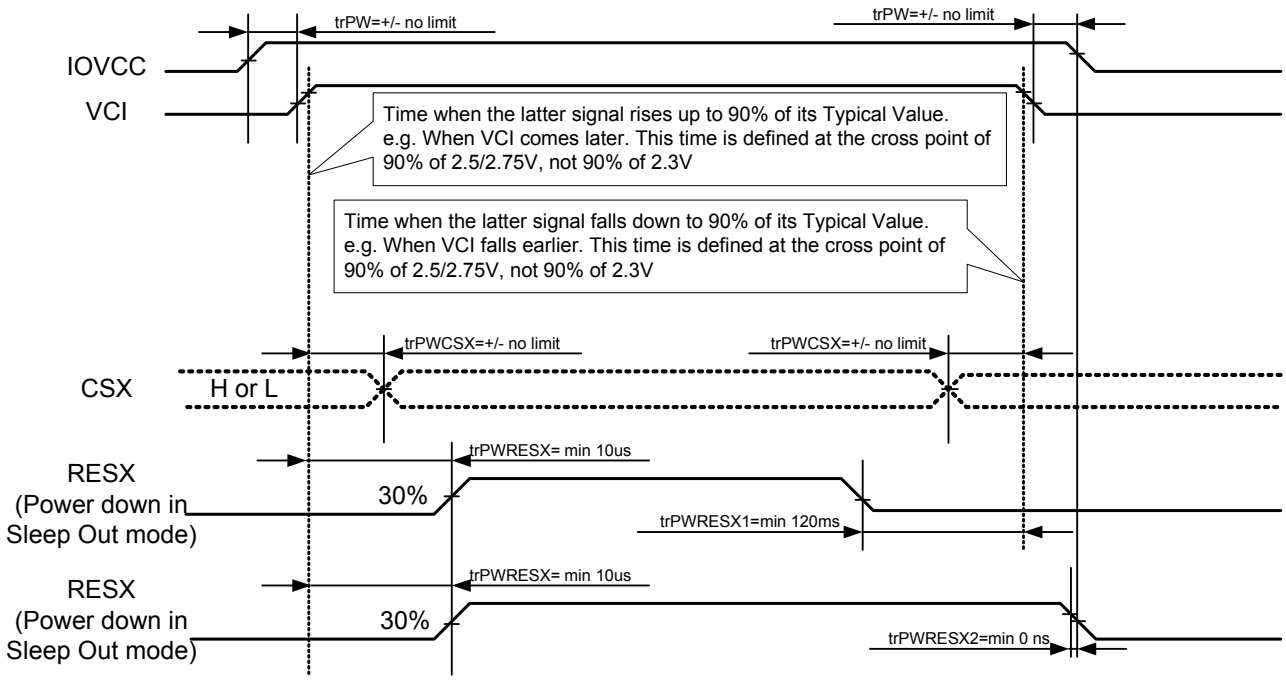


trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9342 will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” actives.

13. Power Level Definition

13.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

   In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

   In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

   In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MPU interface and memory works with IOVCC power supply. Contents of the memory are safe.

6. Deep Standby Mode.

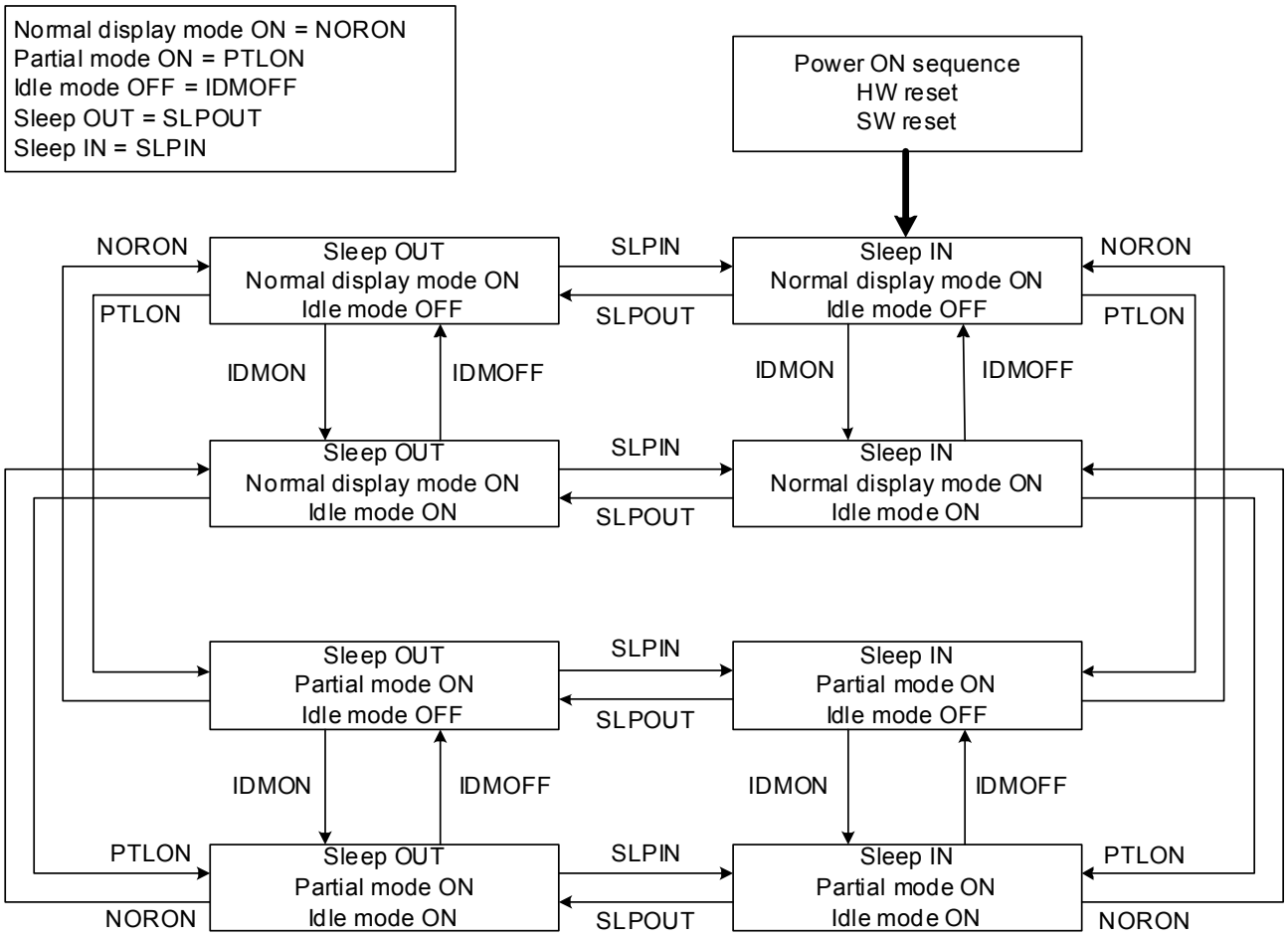
   In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited.

7. Power Off Mode.

   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MPU commands. Mode 6 is entered only when both Power supplies are removed.

13.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

14. Gamma Curves Selection

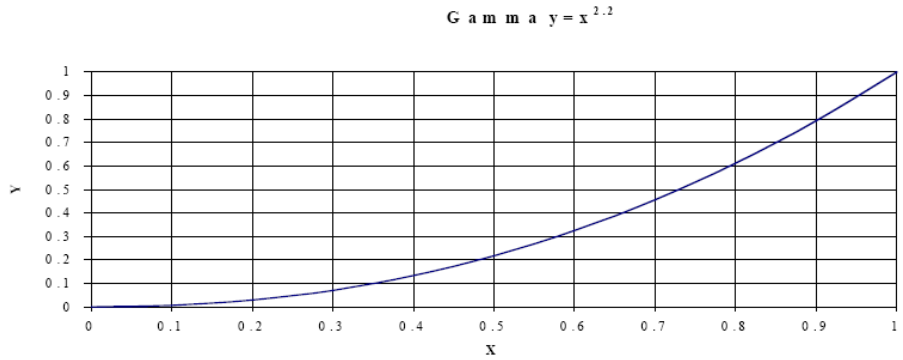
ILI9342 provide four gamma curves (Gamma1.0, Gamma1.8, Gamma2.2 and Gamma2.5). The gamma curve can be selected by the GC0 to GC3 settings.

14.1. Gamma Default Values (for NW type LC)

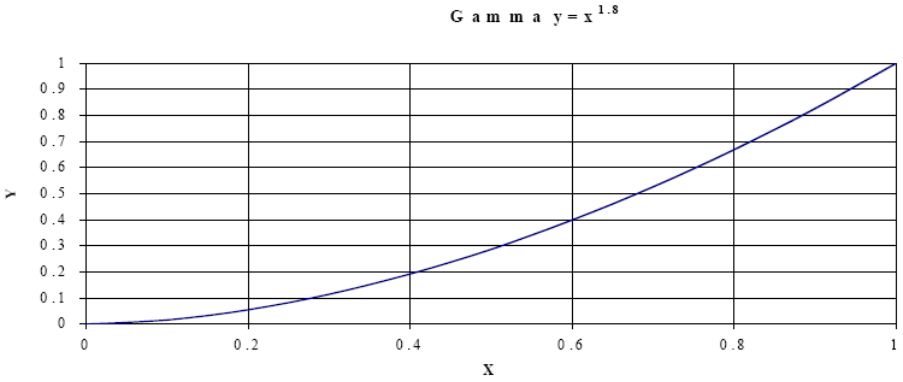
Data	Output Voltage									
	VCOM = Low					VCOM = High				
	Gamma	1.0	1.8	2.2	2.5	Gamma	1.0	1.8	2.2	2.5
0	V0P					V0N				
1	V1P					V1N				
2	V2P					V2N				
3	V3P					V3N				
4	V4P					V4N				
5	V5P					V5N				
6	V6P					V6N				
7	V7P					V7N				
8	V8P					V8N				
9	V9P					V9N				
10	V10P					V10N				
11	V11P					V11N				
12	V12P					V12N				
13	V13P					V13N				
14	V14P					V14N				
15	V15P					V15N				
16	V16P					V16N				
17	V17P					V17N				
18	V18P					V18N				
19	V19P					V19N				
20	V20P					V20N				
21	V21P					V21N				
22	V22P					V22N				
23	V23P					V23N				
24	V24P					V24N				
25	V25P					V25N				
26	V26P					V26N				
27	V27P					V27N				
28	V28P					V28N				
29	V29P					V29N				
30	V30P					V30N				
31	V31P					V31N				
32	V32P					V32N				
33	V33P					V33N				
34	V34P					V34N				
35	V35P					V35N				
36	V36P					V36N				
37	V37P					V37N				
38	V38P					V38N				
39	V39P					V39N				
40	V40P					V40N				
41	V41P					V41N				
42	V42P					V42N				
43	V43P					V43N				
44	V44P					V44N				
45	V45P					V45N				
46	V46P					V46N				
47	V47P					V47N				
48	V48P					V48N				
49	V49P					V49N				
50	V50P					V50N				
51	V51P					V51N				
52	V52P					V52N				
53	V53P					V53N				
54	V54P					V54N				
55	V55P					V55N				
56	V56P					V56N				
57	V57P					V57N				
58	V58P					V58N				
59	V59P					V59N				
60	V60P					V60N				
61	V61P					V61N				
62	V62P					V62N				
63	V63P					V63N				

14.2. Gamma Curves

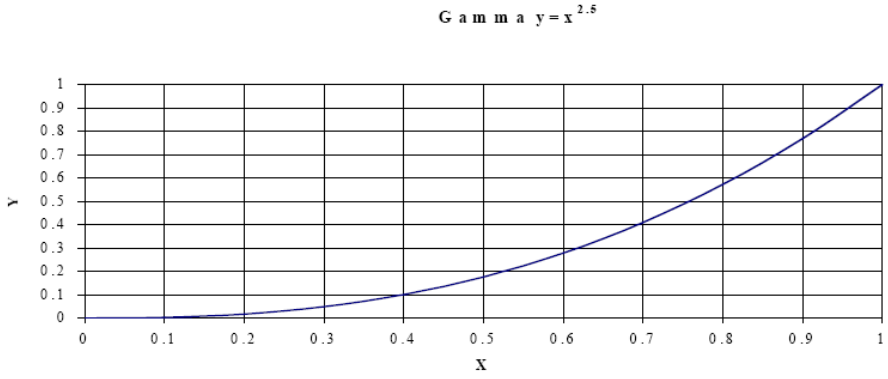
14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



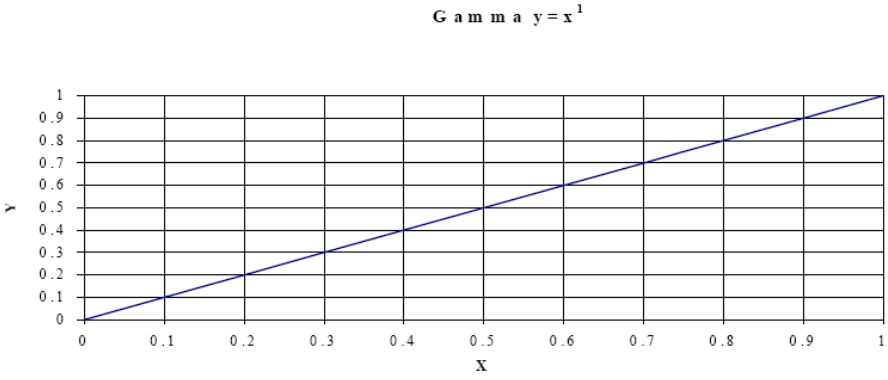
14.2.2. Gamma Curve 2 (GC1), applies the function $y=x^{1.8}$



14.2.3. Gamma Curve 3 (GC2), applies the function $y=x^{2.5}$



14.2.4. Gamma Curve 4 (GC3), applies the function $y=x^{1.0}$



15. Reset

15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	013F h	013F h	If MADCTL's B5=0:013F h If MADCTL's B5=1:00EF h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	00EF h	00EF h	If MADCTL's B5 = 0:00EFh If MADCTL's B5= 1:013F h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	00EF h	00EF h	00EF h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VCI *& IOVCC are applied.*

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Note 4: When a RESX input is entered into the ILI9342 while it is in deep standby mode, the ILI9342 starts up the inside logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable.

15.2. Output Pins, I/O Pins

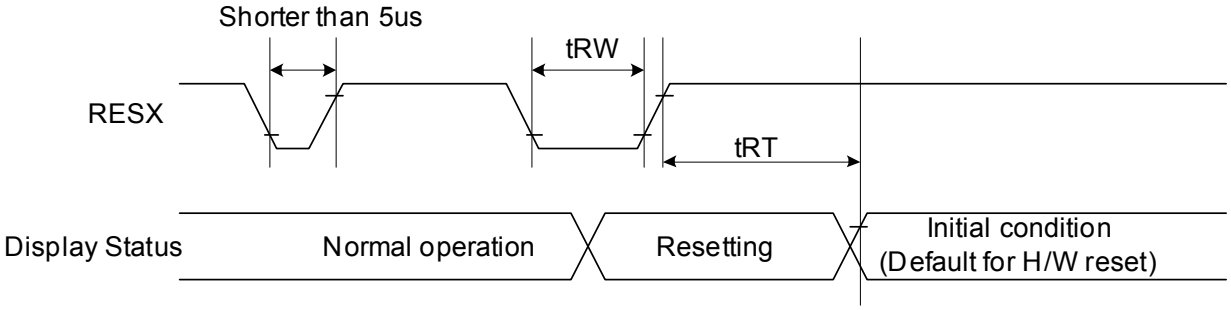
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
DB[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

15.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

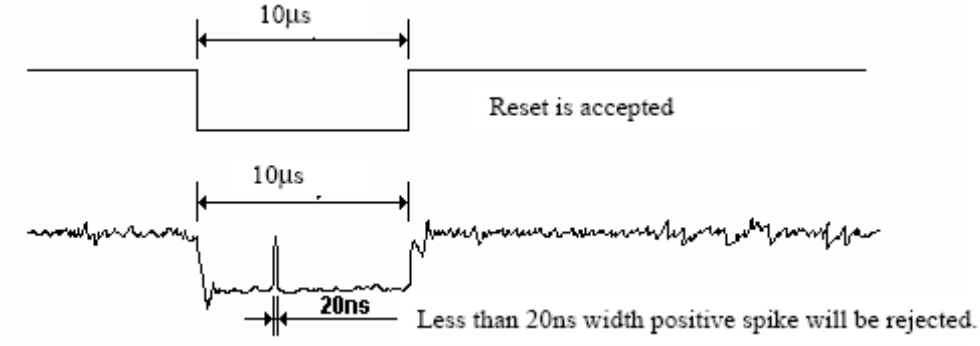
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

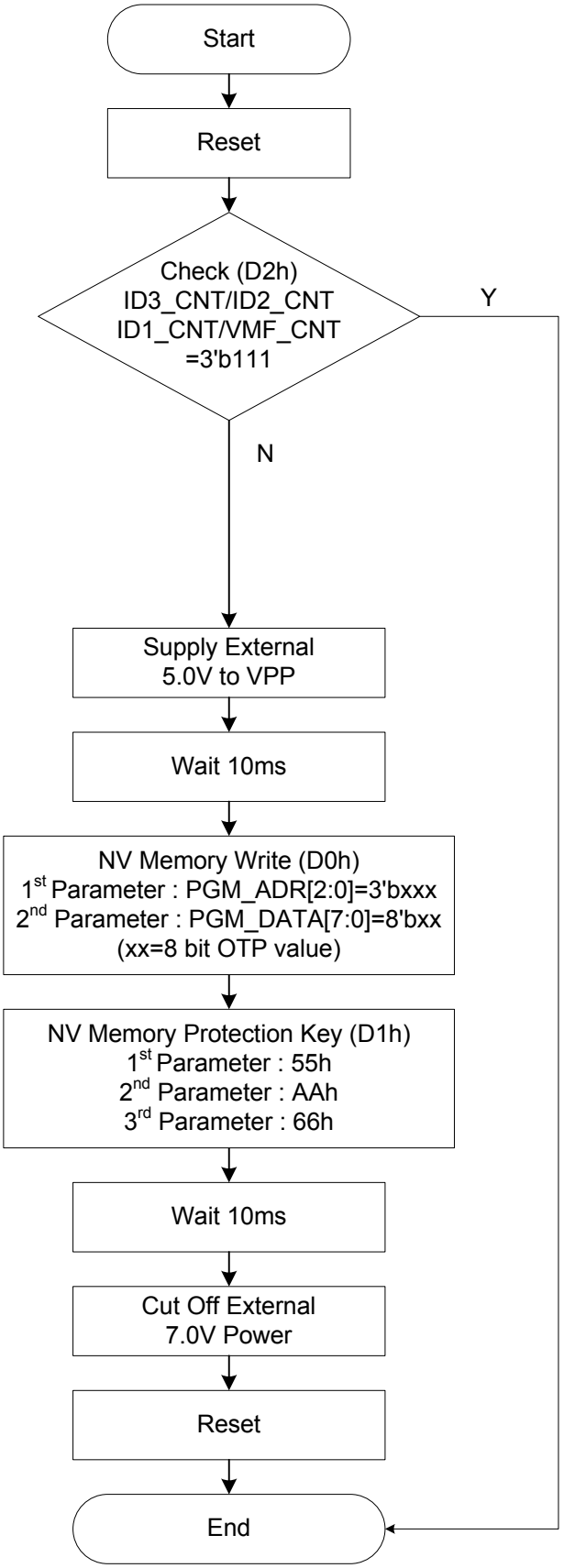


Note 5: When Reset applied during Sleep In Mode.

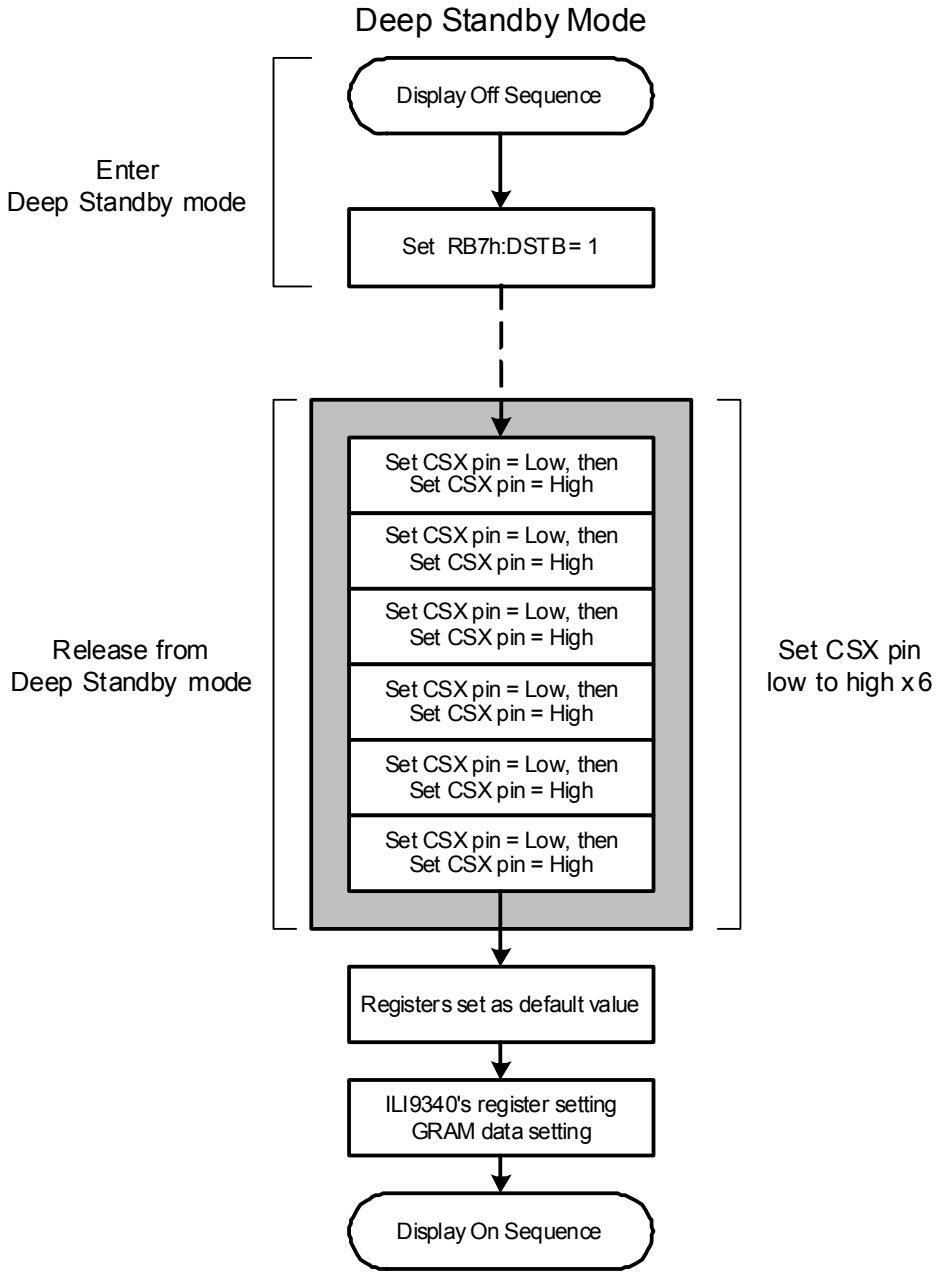
Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

16. NV Memory Programming Flow



17. Deep Standby Mode Setting



Note: (1) To Return display mode according to normal display ON sequence when ILI9342 exits Deep standby mode to Sleep mode.

(2) Leave at lease 1ms between the 2nd and 3rd inputs of CSX=Low.

(3) This sequence must be completed before writing data to GRAM.

(4) ILI9342 exits deep standby mode and enters to sleep mode when an effective RESX pulse is inputted during Deep Standby mode.

18. Electrical Characteristics

18.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9342 is used out of the absolute maximum ratings, ILI9342 may be permanently damaged. To use ILI9342 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9342 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.8
Supply voltage (Logic)	IOVCC	V	-0.3 ~ +3.3
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.4
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ IOVCC + 0.3
Logic output voltage range	VO	V	-0.3 ~ IOVCC + 0.3
Operating temperature	Topr	℃	-40 ~ +85
Storage temperature	Tstg	℃	-55 ~ +110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

18.2. DC Characteristics

18.2.1. General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.3	2.8	4.8	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.8	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	32	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	DGND	-	0.2*IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	DGND	-	0.2*IOVCC	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or DGND	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOM	V	|VCOMH-VCOML|	4.0	-	5.5	Note3
Source Driver							
Source Output Range	Vsout	V	-	0.1	-	DDVDH-0.1	Note4
Gamma Reference Voltage	VREG1OUT	V	-	3.0	-	5.0	Note3

Note 1: IOVCC=1.65 to 3.3V, VCI=2.3 to 4.8V, AGND=DGND=0V, Ta= -40 to 85 °C °C.

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

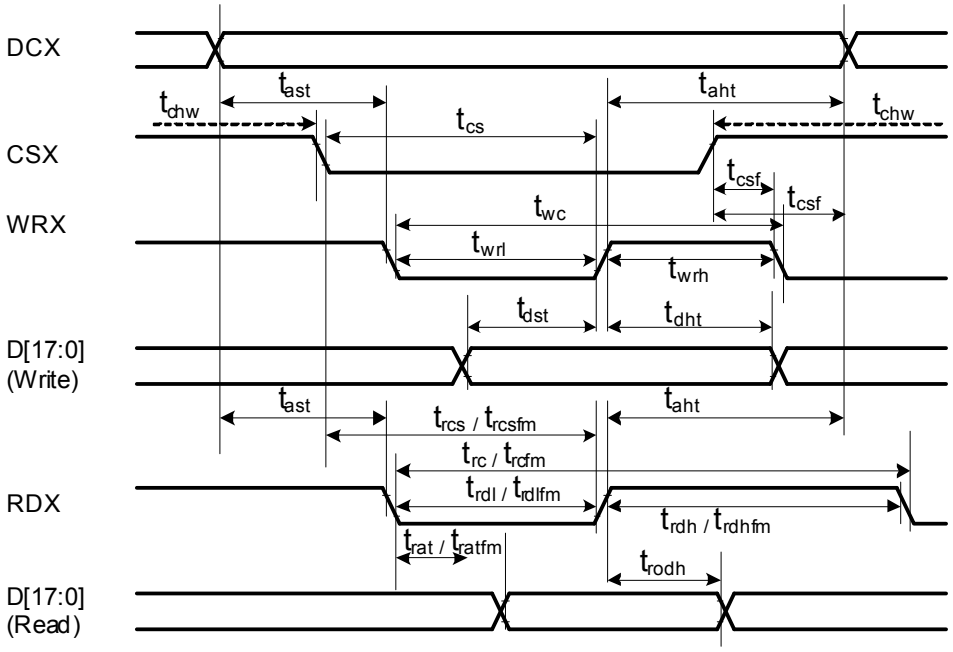
Note3: CSX, RDX, WRX, DB[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

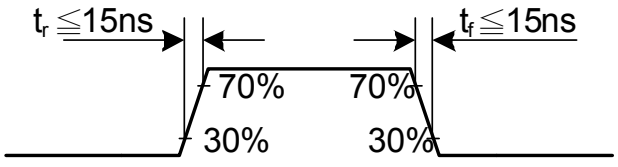
18.3. AC Characteristics

18.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-system)

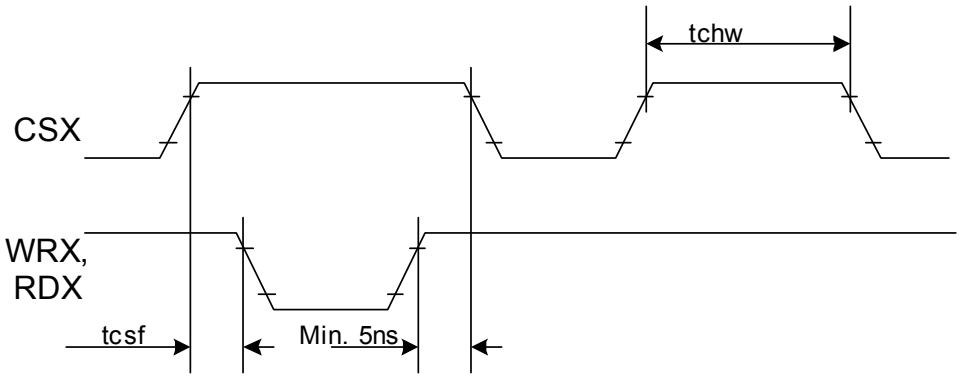


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t_{ast}	Address setup time	0	-	ns	
	t_{hat}	Address hold time (Write/Read)	10	-	ns	
CSX	t_{chw}	CSX "H" pulse width	0	-	ns	
	t_{cs}	Chip Select setup time (Write)	15	-	ns	
	t_{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t_{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t_{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t_{wc}	Write cycle	66		ns	
	t_{wrh}	Write Control pulse H duration	33	-	ns	
	t_{wrl}	Write Control pulse L duration	33	-	ns	
RDX (ID)	t_{rc}	Read cycle (ID)	160	-	ns	When read ID data
	t_{rdh}	Read Control pulse H duration	90	-	ns	
	t_{rdl}	Read Control pulse L duration	45	-	ns	
RDX (FM)	t_{rcfm}	Read Cycle (FM)	450	-	ns	When read from the frame memory
	t_{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t_{rdlfm}	Read Control L duration (FM)	355	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	t_{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t_{dht}	Write data hold time	10	-	ns	
	t_{rat}	Read access time	-	40	ns	
	t_{ratfm}	Read access time	-	340	ns	
	t_{rod}	Read output disable time	20	80	ns	

Note: Ta = -40 to 85 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, DGND=0V

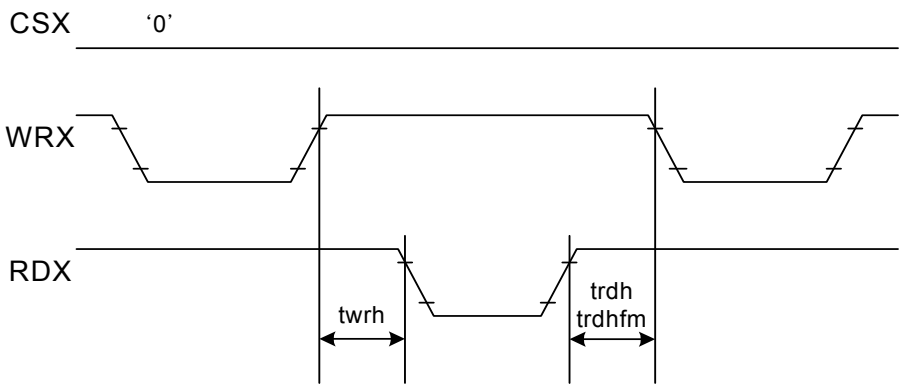


CSX timings :



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

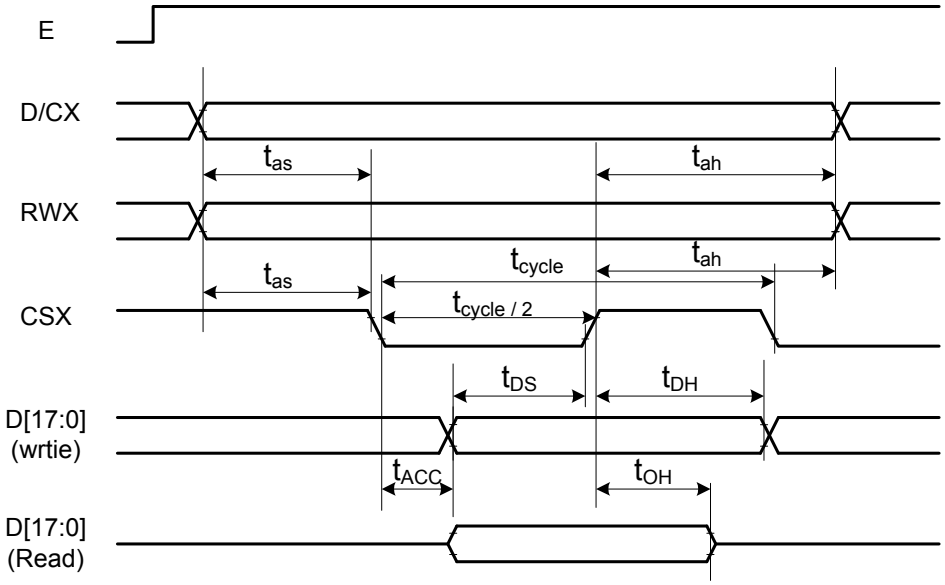


Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

18.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (6800-system)

18.3.3. Fixed E Mode

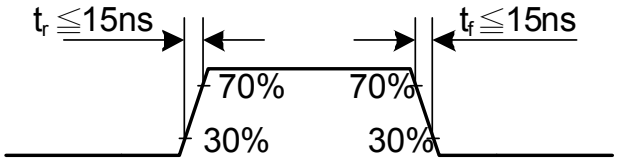
Fixed E Mode



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t_{as}	Address Setup time	10	-	ns	-
	t_{ah}	Address hold Time (Write/Read)	10	-	ns	-
R/WX	t_{as}	Address Setup time	10	-	ns	-
	t_{ah}	Address hold Time (Write/Read)	10	-	ns	-
CSX	t_{cycle}	System Clock Cycle Time	50	790	ns	-
D[23:0]	t_{DS}	Data Setup Time	15	-	ns	-
	t_{DH}	Data Hold Time	25	-	ns	For maximum CL=30pF For minimum CL=8pF
	t_{ACC}	Data Access Time	10	-	ns	
	t_{OH}	Output Hold Time	10	-	ns	

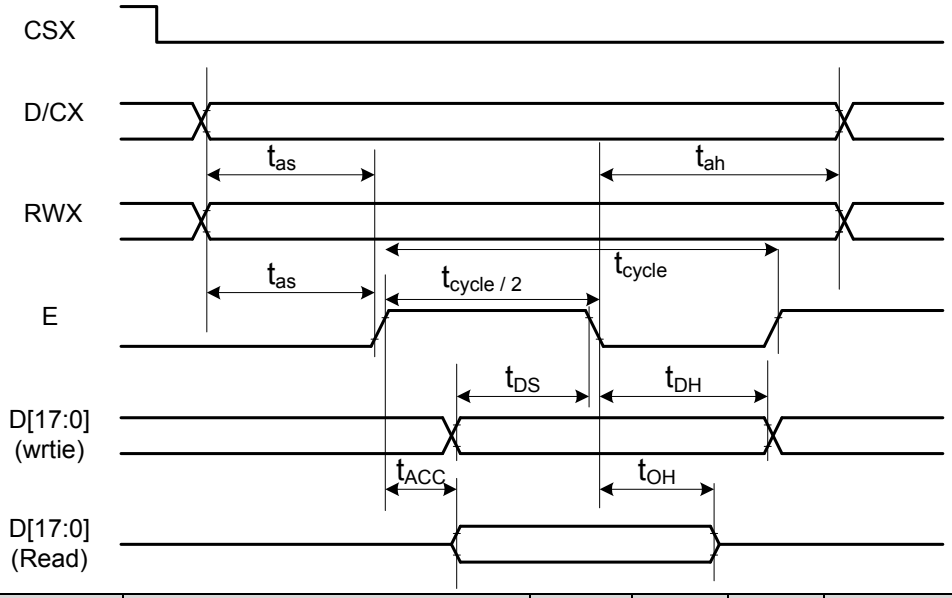
Note: (1) Ta = -40 to 85 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, AGND=DGND=0V

(2) Does not include signal rise and fall times.



18.3.4. Clocked E Mode

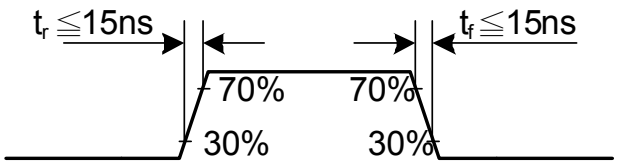
Clocked E Mode



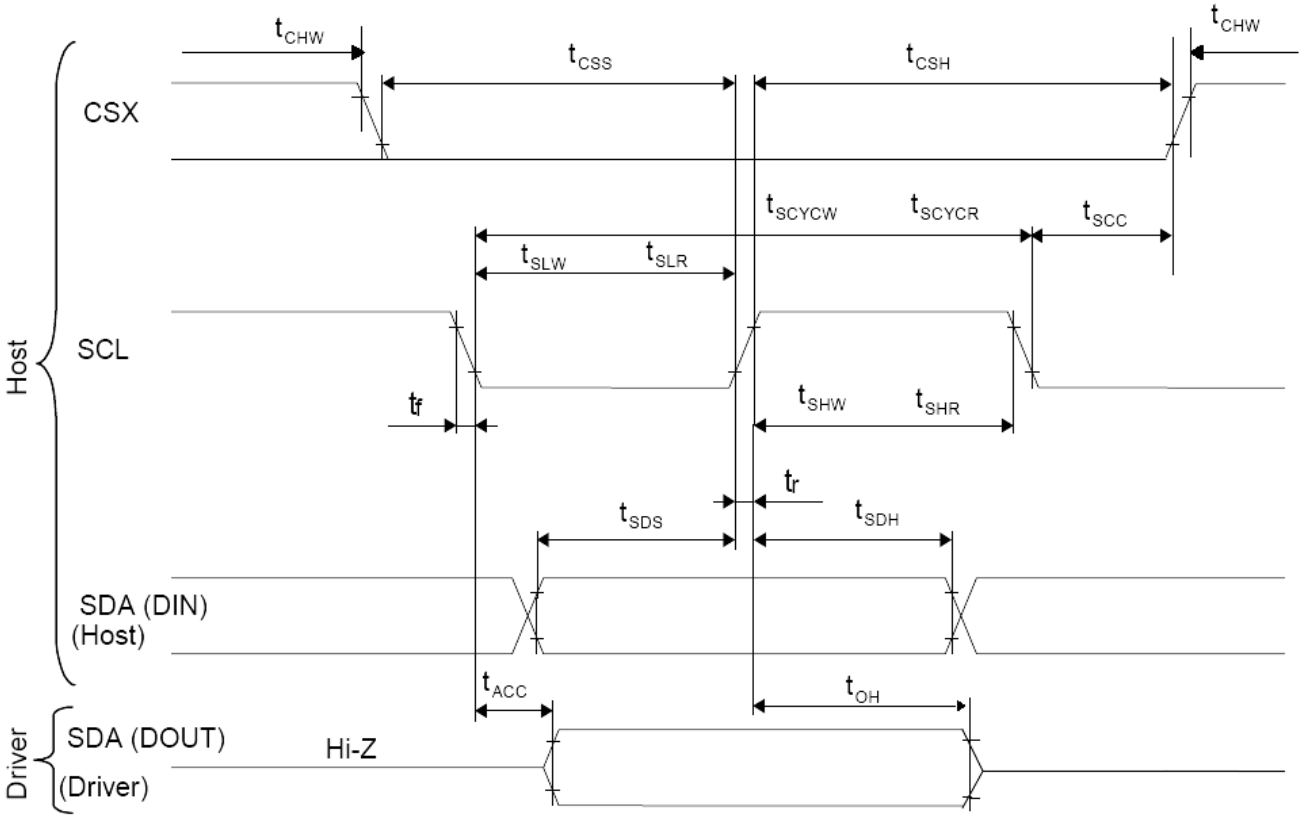
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t_{as}	Address Setup time	10	-	ns	-
	t_{ah}	Address hold Time (Write/Read)	10	-	ns	-
R/WX	t_{as}	Address Setup time	10	-	ns	-
	t_{ah}	Address hold Time (Write/Read)	10	-	ns	-
E	t_{cycle}	System Clock Cycle Time	50	790	ns	-
D[23:0]	t_{DS}	Data Setup Time	15	-	ns	-
	t_{DH}	Data Hold Time	25	-	ns	For maximum CL=30pF For minimum CL=8pF
	t_{ACC}	Data Access Time	10	-	ns	
	t_{OH}	Output Hold Time	10	-	ns	

Note: (1) Ta = -40 to 85 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, AGND=DGND=0V

(2) Does not include signal rise and fall times.

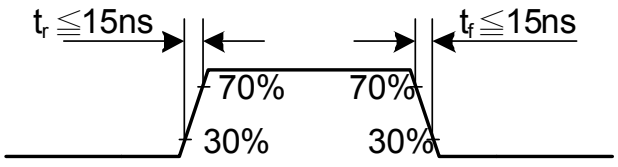


18.3.5. Display Serial Interface Timing Characteristics (3-line SPI system)

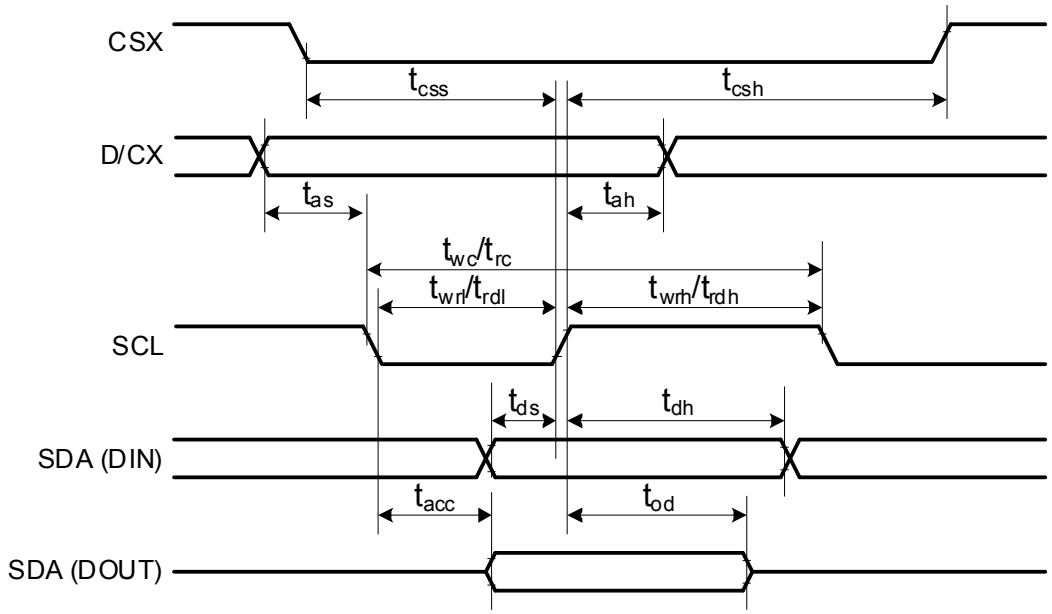


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	t_{scycw}	Serial Clock Cycle (Write)	66	-	ns	
	t_{shw}	SCL “H” Pulse Width (Write)	33	-	ns	
	t_{slw}	SCL “L” Pulse Width (Write)	33	-	ns	
	t_{scycr}	Serial Clock Cycle (Read)	150	-	ns	
	t_{sshr}	SCL “H” Pulse Width (Read)	75	-	ns	
	t_{slr}	SCL “L” Pulse Width (Read)	75		ns	
SDA (Input)	t_{sds}	Data setup time (Write)	10	-	ns	
	t_{sdh}	Data hold time (Write)	10	-	ns	
SDA (Output)	t_{acc}	Access time (Read)	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	t_{oh}	Output disable time (Read)	15	50	ns	For maximum CL=30pF For minimum CL=8pF
CSX	t_{chw}	CSX “H” Pulse Width	40	-	ns	
	t_{scss}	SCL-CSX (Write Time)	15	-	ns	
	t_{csh}		15	-	ns	
	t_{css}	CSX-SCL (ReadTime)	60	-	ns	
	t_{csh}		65	-	ns	

Note: Ta = -40 to 85 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, AGND=DGND=0V

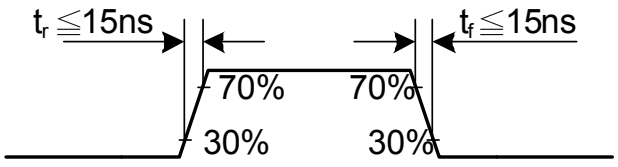


18.3.6. Display Serial Interface Timing Characteristics (4-line SPI system)

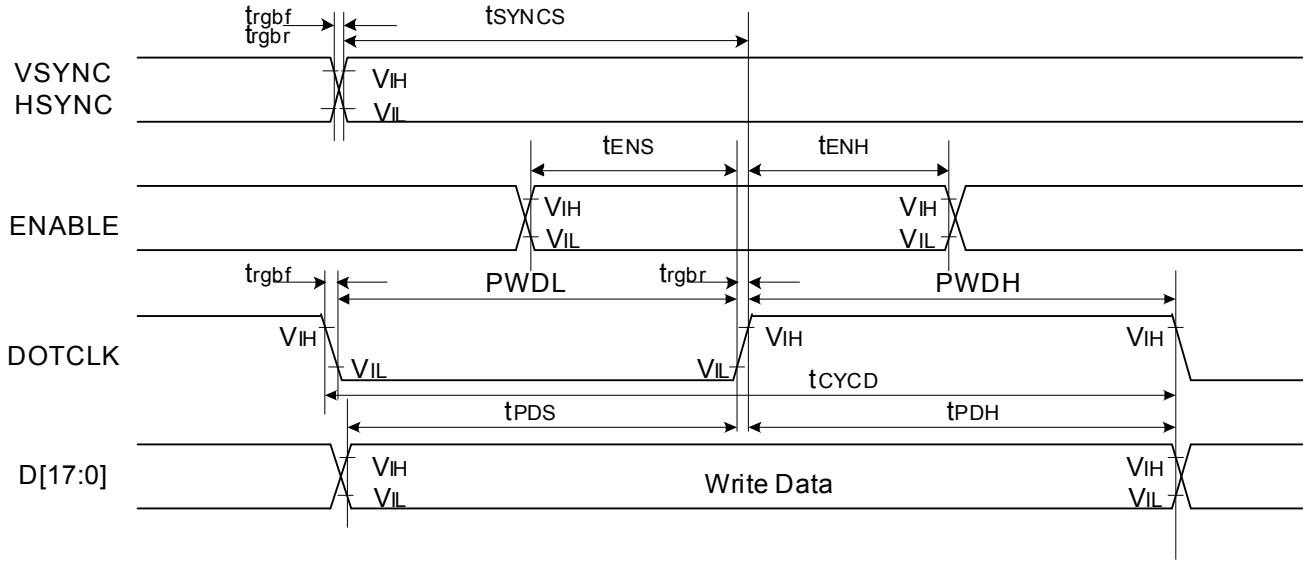


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	15	-	Ns	
	t_{cssh}	Chip select hold time (write)	15	-	Ns	
SCL	t_{wc}	Serial clock cycle (Write)	66	-	Ns	
	t_{wrh}	SCL “H” pulse width (Write)	33	-	Ns	
	t_{wrl}	SCL “L” pulse width (Write)	33	-	Ns	
	t_{rc}	Serial clock cycle (Read)	150	-	Ns	
	t_{rdh}	SCL “H” pulse width (Read)	75	-	Ns	
	t_{rdl}	SCL “L” pulse width (Read)	75	-	Ns	
D/CX	t_{as}	D/CX setup time	10	-	Ns	
	t_{ah}	D/CX hold time (Write / Read)	10	-	Ns	
SDA (Input)	t_{ds}	Data setup time (Write)	10	-	Ns	
	t_{dh}	Data hold time (Write)	10	-	Ns	
SDA (Output)	t_{acc}	Access time (Read)	10	50	Ns	For maximum CL=30pF
	t_{od}	Output disable time (Read)	15	50	Ns	For minimum CL=8pF

Note: Ta = -40 to 85 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, AGND=DGND=0V

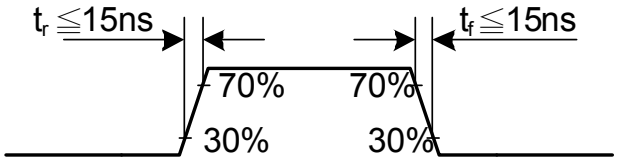


18.3.7. Parallel RGB Interface Timing Characteristics

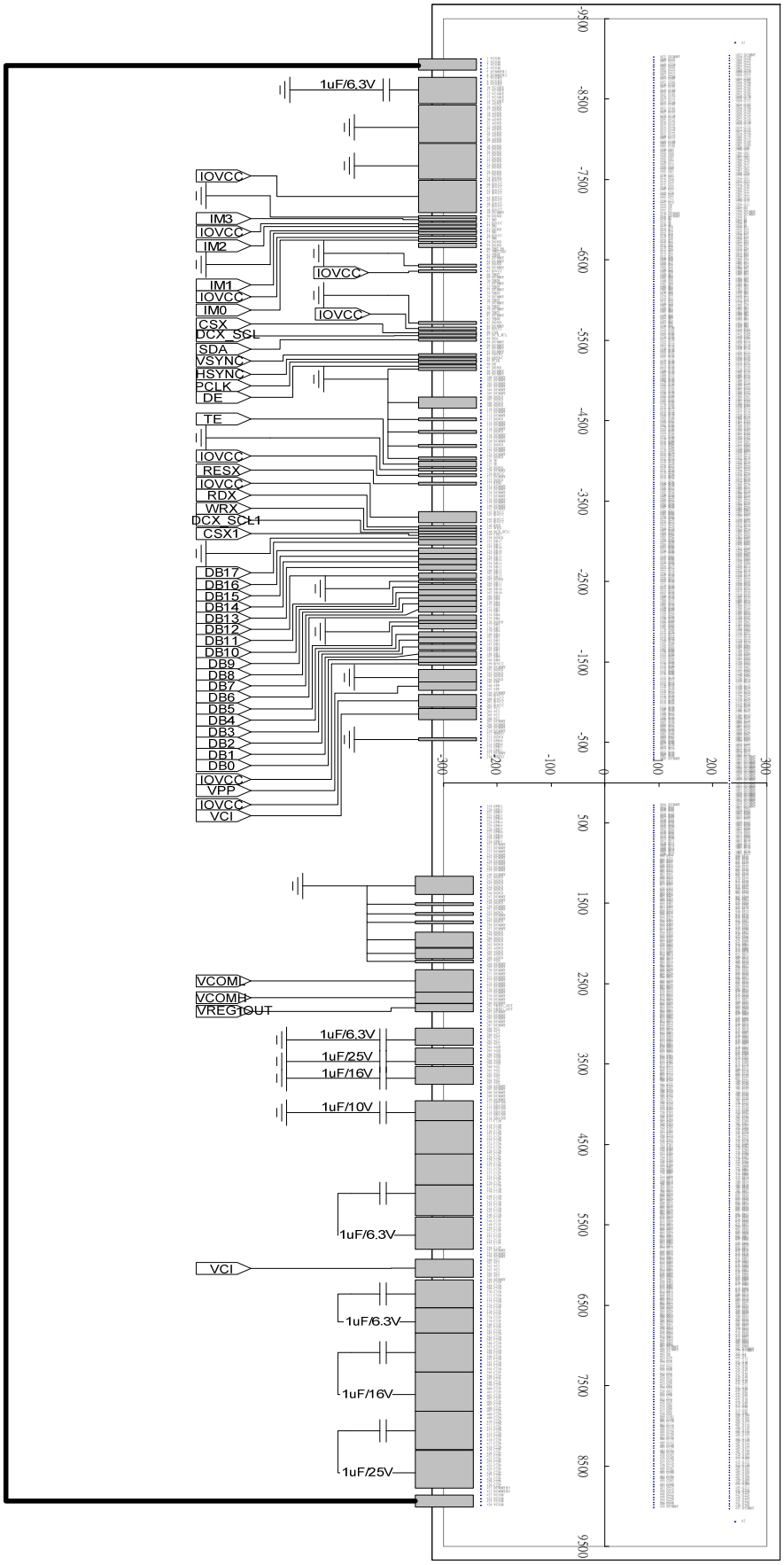


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
DB[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time	66	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
DB[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	33	-	ns	
	PWDL	DOTCLK low-level pulse period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time	66	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -40 to 85 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, AGND=DGND=0V



19. Application Circuit



Items	Recommended Specification	Pin connection
Capacity 1 µF	6.3V	VCORE, VCL, C11P/N, C31P/N, C12P/N (Note 1)
	10V	DDVDH, C21P/N, C22P/N
	16V	VGL
	25V	VGH

Note 1 : If using 3x DDVDH setting , the C12P/N capacity should be add to application circuit.

20. Revision History

Version No.	Date	Page	Description
V001	2009/09/21	All	New Created
V002	2009/12/28	17~25	Pad location table error
V003	2009/12/29	16	Pad size description
V004	2010/2/2	85	Correct Command default
V005	2010/3/3	118	Correct 33h default
		16	Pad diagram
		159	SAP setting correction
V006	2010/3/4	13	Testing description
V007	2010/3/17	9	Circuit block diagram
		12	CSX1/D/CX_SCL1 descriptopn
		215	External capacity value
V008	2010/3/31	99	Modify Sleep out restriction
		150	Modify SS description
		206~213	AC/DC timing revise